Multi-link Gearbox
Implementation Agreement

IA # OIF-MLG-01.0

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IA OIF-MLG-01.0

Working Group: **Physical and Link Layer**

TITLE: **Multi-link Gearbox Implementation Agreement**

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ABSTRACT: The MLG (Multi-Link Gearbox) Project defines a 10:4 Mux MLG function to convert multiple (up to 10) independent 10Gb/s links into 4x25G lanes, and a 4:10 DeMux MLG function to convert the 4x25G lanes back to multiple (up to 10) independent 10Gb/s links.

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5   Introduction

The MLG (Multi-link Gearbox) implementation agreement defines an in-band coding that allows independent 10GBASE-R signals to transit 10:4 gearboxes implementing a 100GBASE-R PMA function. This enables a variety of applications reusing 100GBASE-R technology for the transport of individual 10G links.

A future version of this implementation agreement may provide for the encoding of other 10G link types, e.g., 10GBASE-KR, 10GBASE-W, STM-64, OTU2, and/or OTU2e.

5.1   Requirements

The MLG mux encodes from one to ten 10GBASE-R signals compliant with IEEE Std 802.3-2008 clauses 49 and 51 into a format consistent with the IEEE Std 802.3ba-2010 clause 83 PMA service interface (e.g., four lanes of 25.78125 Gb/s ±100ppm). The MLG demux decodes the format produced by the MLG mux to produce from one to ten 10GBASE-R signals.

The MLG mux to MLG demux link preserves the compliance to IEEE Std 802.3-2008 clauses 49 and 51 of each 10GBASE-R signal. Note that the exact bit sequence of a given 10GBASE-R signal is not preserved across an MLG mux to MLG demux link. The bit sequence may be modified by the insertion and/or deletion of idles and rescrambling. Note also that non-66B formatted 10G signals such as pseudo-random or PRBS cannot transit an MLG link.

The skew and skew variation limits for IEEE 802.3ba-2010 from SP1 to SP6 for a 100GBASE-R PCS lane are met by an MLG mux to MLG demux link.

Operating 10G lanes are not affected by turning on or off any other lane, nor by the failure of any other lane.

An MLG mux to MLG demux link can preserve the long-term average clock frequency of a single selected 10GBASE-R signal, or all signals if they are originally from a common clock source, but how this is achieved is outside the scope of this IA.

5.2   Sample Applications

5.2.1   10GBASE-R Virtual Link

The 10GBASE-R Virtual Link function uses the MLG to transport up to ten (asynchronous) 10GBASE-R signals across a PMD defined for 100GBASE-R, for example, a 100GBASE-LR4 or 100GBASE-ER4 PMD per IEEE Std 802.3ba-2010 clause 88:
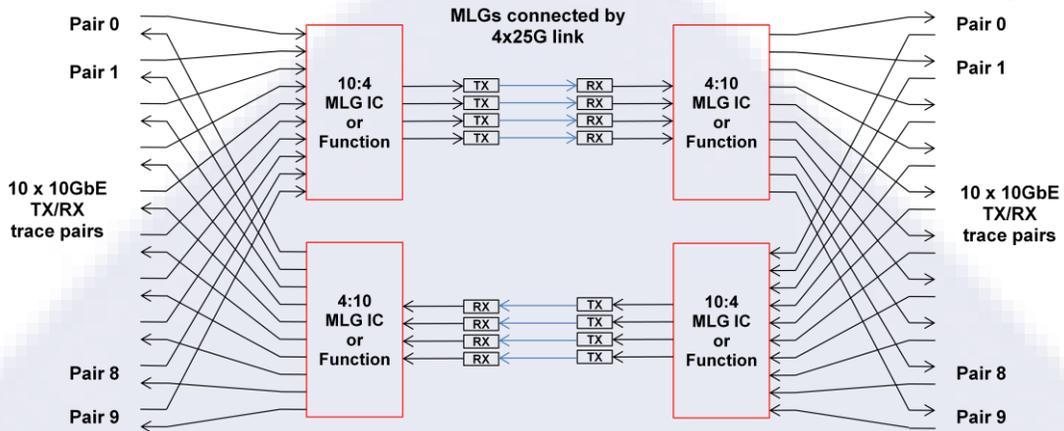
Figure 1: 10GBASE-R Virtual Link

5.2.2   10GBASE-R Port Expander

The 10GBASE-R port expander enables high density 10G I/O using module interfaces, form factors, and higher speed ASIC interfaces designed for 100GBASE-R. This could be applied to electrical or optical interfaces.
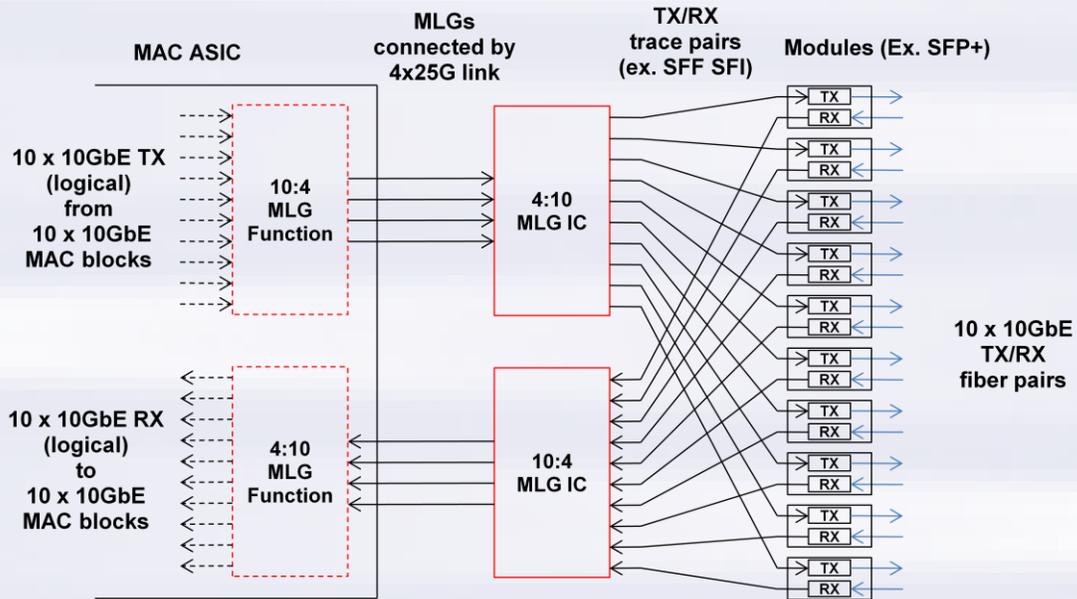

Figure 2: 10GBASE-R Electrical Port Expander
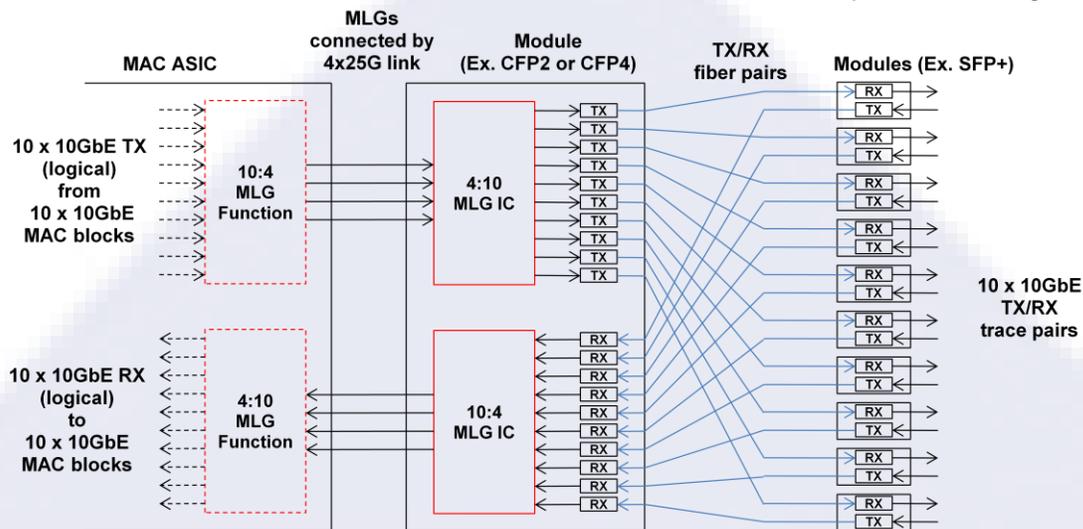
Figure 3: 10GBASE-R Optical Port Expander

6   General Mechanism

The MLG mechanism reuses the 100GBASE-R PMA, which can combine the information from the 100GBASE-R PCS into a variety of different lane widths. The 100GBASE-R PCS is divided into 20 PCS lanes, distributing the 66B blocks of the 103.125 Gb/s aggregate at the PCS Tx round-robin to twenty lanes of 5.15625 Gb/s. Sufficient idles are deleted from the 103.125 Gb/s aggregate bit stream (prior to scrambling and block distribution) to allow for insertion of a 66-bit PCS lane alignment marker after every 16383 66-bit blocks on each PCS lane. The PCS lane alignment markers allow for identification and deskew of the lanes at the Rx end of the link. At the Rx, the lanes are identified, reordered, and deskewed and the lane alignment markers are removed to reassemble the original aggregate sequence of 66-bit blocks. This PCS mechanism is described in IEEE Std 802.3ba-2010 clause 82.

A similar approach is employed by the MLG to transport ten 10GBASE-R signals. Sufficient idles are added or removed from each of the 10GBASE-R signals to map them all to a common clock domain and to make room for the insertion of the 66-bit MLG lane alignment markers described below. Each 10GBASE-R signal is then demultiplexed into two MLG lanes (running at 5.15625 Gb/s) by alternating 66-bit blocks on each of the two lanes. A 66-bit MLG lane alignment (and identification) marker is simultaneously inserted on each of these MLG lanes after every 16383 66-bit blocks. The MLG lanes are identified as lane x.y, where x=0 to 9 indicates which of the ten 10GBASE-R signals is being carried, and y=0 or 1 identify the two MLG lanes that comprise a particular 10GBASE-R signal.

At the MLG demux, the MLG lanes are identified, deskewed, reordered, and the MLG lane alignment markers removed. Pairs of MLG lanes comprising each 10GBASE-R signal are reinterleaved on a 66-bit block basis. Idles can then be added or removed from each 10GBASE-R signal to map it onto a new 10G output clock domain (if required).

6.1   MLG Lane Markers

The twenty MLG lane marker values are chosen for MLG so as not to replicate the values used in the 100GBASE-R PCS or 40GBASE-R PCS. This will prevent accidental

interconnection of an MLG formatted signal with a 100GBASE-R PCS from trying to bring up a link.

Table 1: MLG Lane Alignment Marker Values

MLG lane number	Encoding[a] {M0, M1, M2, BIP$_3$, M4, M5, M6, BIP$_7$}	MLG lane number	Encoding[a] {M0, M1, M2, BIP$_3$, M4, M5, M6, BIP$_7$}
0.0	0x80, 0xB4, 0xAF, BIP$_3$, 0x7F, 0x4B, 0x50, BIP$_7$	0.1	0x29, 0x85, 0x1D, BIP$_3$, 0xD6, 0x7A, 0xE2, BIP$_7$
1.0	0x11, 0x2A, 0xD8, BIP$_3$, 0xEE, 0xD5, 0x27, BIP$_7$	1.1	0xBF, 0x7E, 0x4D, BIP$_3$, 0x40, 0x81, 0xB2, BIP$_7$
2.0	0x7C, 0x3F, 0x1C, BIP$_3$, 0x83, 0xC0, 0xE3, BIP$_7$	2.1	0xEE, 0x8B, 0xBA, BIP$_3$, 0x11, 0x74, 0x45, BIP$_7$
3.0	0xD1, 0x87, 0x25, BIP$_3$, 0x2E, 0x78, 0xDA, BIP$_7$	3.1	0xD0, 0x02, 0x39, BIP$_3$, 0x2F, 0xFD, 0xC6, BIP$_7$
4.0	0x6D, 0xFE, 0x11, BIP$_3$, 0x92, 0x01, 0xEE, BIP$_7$	4.1	0xA1, 0xD2, 0xAB, BIP$_3$, 0x5E, 0x2D, 0x54, BIP$_7$
5.0	0x0E, 0xC6, 0x3C, BIP$_3$, 0xF1, 0x39, 0xC3, BIP$_7$	5.1	0x98, 0x78, 0x07, BIP$_3$, 0x67, 0x87, 0xF8, BIP$_7$
6.0	0x1B, 0xBF, 0xA0, BIP$_3$, 0xE4, 0x40, 0x5F, BIP$_7$	6.1	0x31, 0x90, 0xC3, BIP$_3$, 0xCE, 0x6F, 0x3C, BIP$_7$
7.0	0x0D, 0x9A, 0x46, BIP$_3$, 0xF2, 0x65, 0xB9, BIP$_7$	7.1	0x9F, 0x08, 0xB6, BIP$_3$, 0x60, 0xF7, 0x49, BIP$_7$
8.0	0xBB, 0x55, 0x9D, BIP$_3$, 0x44, 0xAA, 0x62, BIP$_7$	8.1	0xA8, 0x05, 0xFC, BIP$_3$, 0x57, 0xFA, 0x03, BIP$_7$
9.0	0x04, 0xA1, 0x94, BIP$_3$, 0xFB, 0x5E, 0x6B, BIP$_7$	9.1	0x07, 0x72, 0xDB, BIP$_3$, 0xF8, 0x8D, 0x24, BIP$_7$

7 **Detailed Block Diagrams**

The detailed processing to implement the functionality described in clause 6 is provided in this clause.

7.1 MLG mux

The block diagram for the MLG mux is shown in Figure 4.
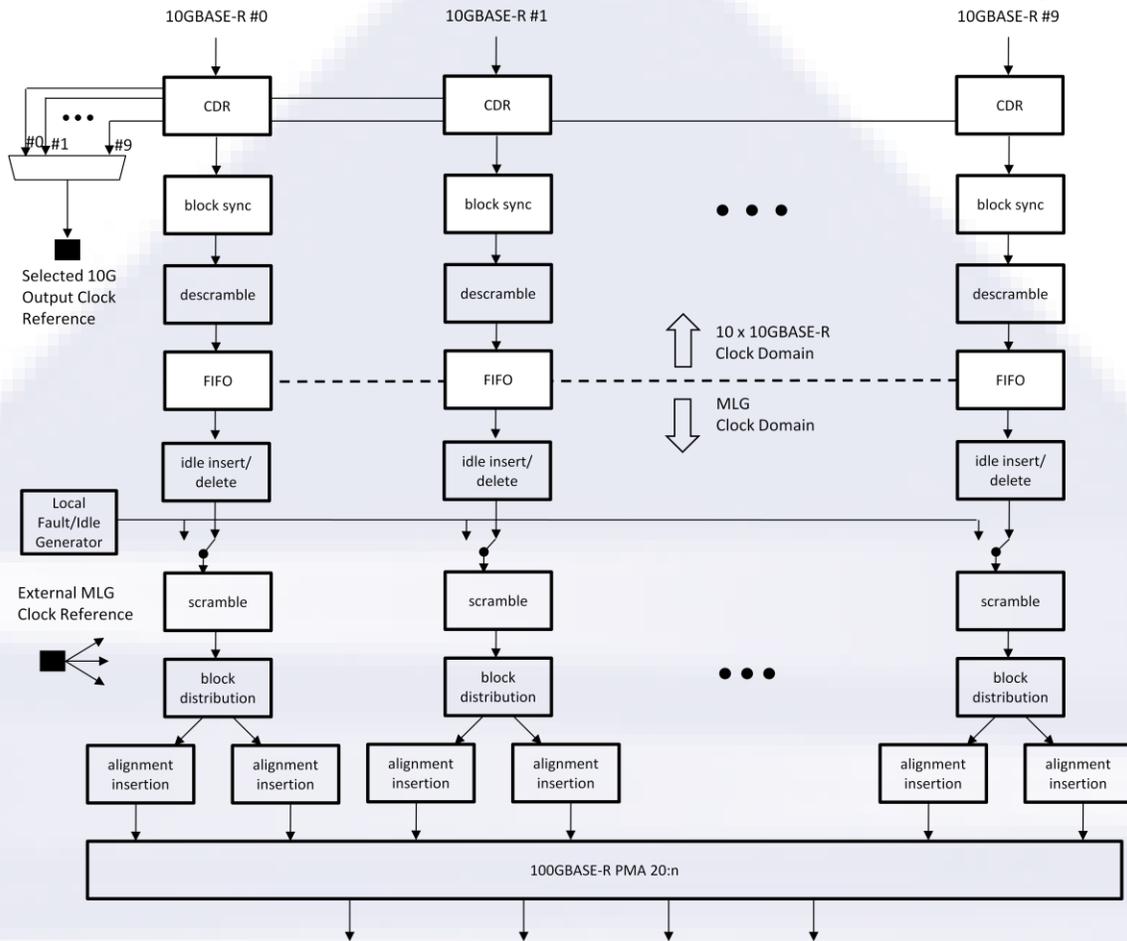
Figure 4: MLG mux Block Diagram

7.1.1   Clock and Data Recovery (CDR)

Each of the ten input 10GBASE-R signals to the MLG mux will undergo clock and data recovery. This function also provides input to the signal detect function which is used to indicate failure of the input signal to the management interface and downstream functions. One of the recovered 10GBASE-R clocks can also be selected to be output as a 10G timing reference, and used (if required) to drive a network timing architecture such as SyncE.

7.1.2   Block Sync

Once clock and data has been recovered from a 10GBASE-R signal, 66B block synchronization is obtained. This is done per the state diagram in Figure 49-12 of IEEE Std 802.3-2008. When block lock=false per this state diagram, this is considered a failure of the input signal equivalent to not being able to recover clock and data as part of the signal detect function.

7.1.3   Descramble

The non-sync header bits of the 10GBASE-R signal are descrambled using the process as described in clause 49.2.10 of IEEE Std 802.3-2008.

7.1.4 Idle Insert/Delete

Idles are inserted or deleted as necessary in order that the bitstream, after lane marker insertion, will match a common MLG clock reference. Idle insertion and deletion shall comply with the rules defined in IEEE Std 802.3-2008 clause 48.2.4.2.3.

An external MLG clock reference is provided as an input to the MLG mux block. The external MLG clock reference may be sourced from either a local free-running oscillator (± 100ppm), or from a system level BITS/SyncE timing architecture. The exact implementation of the external MLG clock reference is a system architecture decision, and outside the scope of this IA.

7.1.5 Local Fault (LF) Insertion

If the incoming 10GBASE-R signal is disabled or has failed (see the signal detect function as part of CDR in 7.1.1), the signal will be replaced with an Ethernet Local Fault sequence ordered set. This is a 66B block with the contents: Sync Header=10; Control block type=0x55; O1=0x0; O4=0x0; and the local fault encoding indicated in Table 46-5 of IEEE Std 802.3-2008 in D_1, D_2, D_3 and D_5, D_6, D_7. There should be sufficient buffer to allow replacement of a failed incoming signal with Local Fault without interruption to the traffic in the other 10GBASE-R signals: for example, if there is not a full 66B block available for transmission, the Local Fault control block will be transmitted instead, maintaining the 66B block alignment with the data it replaces.

7.1.6 Scrambled Idle Test Pattern Generation

The MLG mux may optionally generate for each lane a scrambled idle test pattern. This test pattern can traverse a gearbox, and can be checked by the far-end MLG demux, or looped back at the MLG demux or Ethernet Rx and checked at the near end MLG demux. An MLG implementation that includes this capability shall perform it as described in this clause

When a scrambled idle pattern is enabled for a given 10G signal, it shall be generated at the input to the scrambler (see 7.1.7). The input to the scrambler is a control block (block type=0x1E) with all idles as defined in IEEE Std 802.3ba-2010 Figure 82–5. When switching between scrambled idle test pattern mode and normal operation, the 66B block alignment shall be maintained.

7.1.7 Scramble

After idle insertion/deletion and Local Fault insertion if necessary, the resulting stream is re-scrambled. This is done according to clause 49.2.6 of IEEE Std 802.3-2008.

7.1.8 Block Distribution

The 66B blocks of each 10GBASE-R signal are distributed to two MLG lanes, alternating 66B blocks on each lane. This is a similar process to that described in clause 82.2.6 of IEEE Std 802.3ba-2010, but distributing to two lanes rather than four or ten lanes.

7.1.9 Alignment Marker Insertion

In order to support deskew and reordering of the MLG lanes into the constituent 10GBASE-R signals at the MLG demux, alignment markers are added periodically to each MLG lane. Each alignment marker is a special 66B block. The alignment markers shall be inserted after every 16383 data blocks on each MLG lane in the same way (at the same time on all twenty MLG lanes) as the insertion of PCS lane alignment markers

described in clause 82.2.7 of IEEE Std 802.3ba-2010. The alignment marker values are given in Table 1. These values are distinct from the PCS lane alignment markers used for 40GBASE-R and 100GBASE-R signals, so there is no possibility to accidentally frame ten 10GBASE-R signals as a 100GBASE-R or vice-versa. The BIP_3 and BIP_7 fields of each lane alignment marker are calculated over all of the previous bits on the given MLG lane, from and including the previous lane alignment marker but not the current lane alignment marker per the procedures described for PCS lanes in clause 82.2.8 of IEEE Std 802.3ba-2010.

7.1.10   100GBASE-R PMA(20:n)

The processes described in clauses 7.1.1 through 7.1.9 will produce twenty MLG lanes, each with a bit rate of 5.15625 Gb/s ±100ppm (all MLG lanes locked to the common clock source). These MLG lanes can now be combined as if they were 100GBASE-R PCS lanes using the 100GBASE-R PMA into any physical lane configuration used to support 100GBASE-R. The most typical value of "n" is expected to be 4 for the MLG application. A PMA(20:4) will produce a 4-lane by 25.78125 Gb/s interface, where each of these physical lanes carries five of the twenty MLG lanes, bit multiplexed. Note that an implementation may support generation of any of the optional test patterns specified for a 100GBASE-R PMA across the MLG link: see IEEE Std 802.3ba-2010 clause 83.5.10. If supported, the corresponding MDIO control variables must also be supported.

7.1.11   MLG mux Management

Control Variables:

- MLG_mux_Enable – Enables or disables the MLG function output
- MLG_mux_10G_Enable_0 through MLG_mux_10G_Enable_9 – Enables or disables each of the 10G lanes. Any disabled lane will have Local Fault inserted as described in 0.
- MLG_mux_10G_Output_Timing_Reference – Selects which of the 10GBASE-R signals provides the 10G timing output reference.
- MLG_mux_scrambled_idle_enable_0 through MLG_mux_scrambled_idle_enable_9 – if implemented, enables or disables the scrambled idle test pattern generated on a given 10G lane

Status Variables:

- Signal_Detect_0 through Signal_Detect_9 – Indicates whether a 10GBASE-R signal was successfully recovered through CDR and the 66B block lock process on each of the input lanes.
- MLG_mux_scrambled_idle_ability – Indicates whether this implementation of MLG has the ability to generate the 10G scrambled idle test pattern on each 10G lane.

7.2   MLG demux

The block diagram for the MLG demux is given in Figure 5.
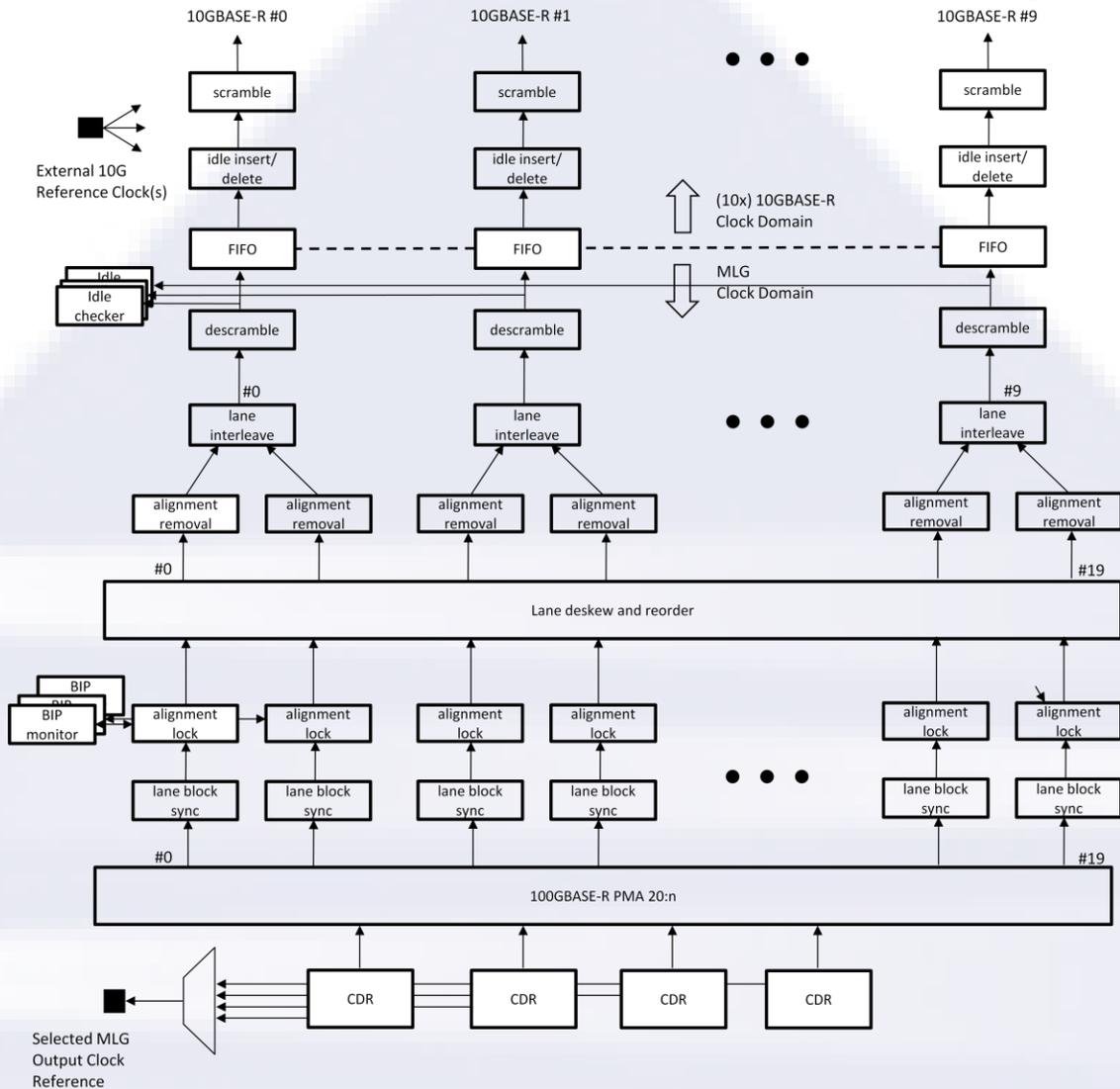
Figure 5: MLG demux Block Diagram

7.2.1   100GBASE-R PMA(20:n)

The input to the MLG mux will come from a physical interface that is similar to that of 100GBASE-R. For the most common MLG configuration, this is expected to be a 4-lane by 25.78125 Gb/s interface, where each of these physical lanes carries five of the twenty MLG lanes, bit multiplexed, but other lane counts which are divisors of 20 are possible. The PMA(n:20) will demultiplex the MLG lanes as if they were PCS lanes into twenty individual bit streams of 5.15625 Gb/s ±100ppm. Note that an implementation may support detection of any of the optional test patterns specified for a 100GBASE-R PMA across the MLG link: see IEEE Std 802.3ba-2010 clause 83.5.10. If supported, the corresponding MDIO control and status variables must also be supported.

7.2.2   Lane block sync

66B block sync is obtained on each of the MLG lanes in the same manner as 100GBASE-R PCS lanes using the state diagram in Figure 82-10 of IEEE Std 802.3ba-2010.

7.2.3   Alignment lock

Alignment marker lock is obtained on each MLG lane in the same manner as 100GBASE-R PCS lanes using the state diagram in Figure 82-11 of IEEE Std 802.3ba-2010, using the expected lane alignment marker values from Table 1.

7.2.4   BIP monitor

The expected BIP value is compared to the received BIP value in each received alignment marker and BIP error counters for each MLG lane are incremented as described for PCS lanes in clause 82.2.14 of IEEE Std 802.3ba-2010.

7.2.5   Lane reorder

Once alignment marker lock has been obtained on the two MLG lanes that comprise a 10GBASE-R signal, those lanes are deskewed, reordered and the 66B blocks interleaved to reconstitute the original 10GBASE-R signal.

7.2.6   Alignment removal

The alignment markers in each MLG lane are removed in the same way as for 100GBASE-R PCS lane alignment markers described in clause 82.2.14 of IEEE Std 802.3ba-2010.

7.2.7   Lane Interleave

The pairs of MLG lanes comprising each 10GBASE-R signal being carried over the MLG link, are 66B block interleaved to reconstitute the original 10GBASE-R signals.

7.2.8   Descramble

The non-sync header bits of the 10GBASE-R signal are descrambled using the process as described in clause 49.2.10 of IEEE Std 802.3-2008.

7.2.9   Scrambled Idle Test Pattern Checker

The MLG mux may optionally implement a scrambled idle test pattern checker for each 10GBASE-R signal. If implemented, it shall be as described in this clause.

When align_status is true and the scrambled idle receive test-pattern mode is active, the scrambled idle test-pattern checker observes the sync header and the output from the descrambler. When the sync header and the output of the descrambler is the all idle pattern, a match is detected. When operating in scrambled idle test pattern, the test-pattern error counter counts blocks with a mismatch. Any mismatch indicates an error and shall increment the test-pattern error counter. Due to the error multiplication characteristics of the descrambler, the incoming bit error ratio can be estimated by dividing the 66-bit block error ratio by a factor of 124.

7.2.10   Idle Insert/Delete

Idles are inserted or deleted as necessary to map the rate of each 10GBASE-R signal to the required 10G output clock rate. Idle insertion and deletion shall comply with the rules defined in IEEE Std 802.3-2008 clause 48.2.4.2.3.

Note, each 10GBASE-R signal can in theory be mapped to an independent 10G output clock domain, driven by an external 10G clock reference. The external 10G reference clock(s) may be sourced from either a local, free-running oscillator (±100ppm), or from a

system/network level BITS/SyncE timing architecture. The exact implementation of the external 10G reference clock(s) for a given application is a system architecture decision, and outside the scope of this IA.

However for reference it is noted that a BITS/SyncE timing architecture can be used to allow a timing reference from one of the 10GBASE-R input signals to be carried across a MLG link (and used to clock one or more of the 10GBASE-R output signals).

7.2.11 Scramble

After idle insertion/deletion, each 10GBASE-R signal is re-scrambled according to clause 49.2.6 of IEEE Std 802.3-2008.

7.2.12 MLG demux Management

Control variables:

- MLG_demux_10G_Enable_0 through MLG_demux_10G_Enable_9 – Enables or disables each of the 10G output lanes.
- MLG_demux_scrambled_idle_enable_0 through MLG_demux_scrambled_idle_enable_9 – if implemented, enables or disables the scrambled idle test pattern checker for the indicated 10G lane.

Status variables:

Note that MLG lanes may be received by the MLG demux on different lanes than those on which they were originally transmitted by the MLG mux due to skew between lanes and multiplexing by the intervening 100GBASE-R PMA(s). Prior to the lane reorder block, MLG lanes are known simply by the position 0..19 on which they were received. After alignment lock on all lanes and lane reorder, MLG lanes are known by which half of which 10GBASE-R signal they represent (0.0, 0.1, 1.0, …, 9.1).

- MLG_demux_Link_Status – indicates whether the input lanes of the MLG demux are being received at the PMA(n:20). Depending on n, individual lane status variables may be available. Since n is implementation dependent, so are the status registers.
- block_lock_0 through block_lock_19 – indicate whether 66B block lock has been achieved on each of the MLG lanes
- am_lock_0 through am_lock_19 – indicates whether alignment marker lock has been achieved on each of the MLG lanes
- MLG_demux_lane_alignment_status – indicates whether all 20 lanes have achieved lane alignment marker lock, that the 20 distinct lane markers are received, and inter-MLG lane skew permits the 10GBASE-R signals to be reassembled.
- BIP_error_counter_0 through BIP_error_counter_19 – contains the count of BIP errors counted on each MLG lane.
- lane_0_mapping through lane_19_mapping – indicates which (logical) MLG lane is received in each MLG lane position. Note that the MLG lanes that may be received in a MLG lane position are numbered 0.0, 0.1, 1.0, …, 9.1.
- MLG_demux_scrambled_idle_ability – indicates whether this implementation implements the optional scrambled idle pattern checker in the MLG demux
- MLG_demux_scrambled_idle_error_0 through MLG_demux_scrambled_idle_error_9 – When the test pattern checker is

enabled, counts the pattern mismatches on the indicated 10GBASE-R signal. The counter is reset to zero at the point that the test pattern checker is enabled.

7.3   Generic MLG Management

Control Variables:

- MLG_10G_loopback_enable_0 through MLG_10G_loopback_enable_9: When enabled, loops back the 10GBASE-R signal recovered on the given 10G output interface at the MLG demux to the corresponding 10G input interface at the MLG mux.

8   References

8.1   Normative references

[1] IEEE Std 802.3-2008 Part 3: Carrier sense multiple access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications.

[2] IEEE Std 802.3ba-2010: Amendment 4: Media Access Control Parameters, Physical Layers, and Management Parameters for 40 Gb/s and 100 Gb/s Operation

9   Appendix A: List of companies belonging to OIF when document is approved

Acacia Communications	FCI USA LLC	MoSys, Inc.
ADVA Optical Networking	Fiberhome Technologies Group	NEC
Alcatel-Lucent	Finisar Corporation	NeoPhotonics
Altera	France Telecom Group/Orange	Nokia Siemens Networks
AMCC	Fujitsu	NTT Corporation
Amphenol Corp.	Fundacao.CPqD	Oclaro
Anritsu	Furukawa Electric Japan	Opnext
Applied Communication Sciences	GigOptix Inc.	PETRA
AT&T	Hewlett Packard	Picometrix
Avago Technologies Inc.	Hitachi	PMC Sierra
Broadcom	Hittite Microwave Corp	QLogic Corporation
Brocade	Huawei Technologies	Reflex Photonics
Centellax, Inc.	IBM Corporation	Semtech
China Telecom	Infinera	SHF Communication Technologies
Ciena Corporation	Inphi	Sumitomo Electric Industries
Cisco Systems	IP Infusion	Sumitomo Osaka Cement
ClariPhy Communications	JDSU	TE Connectivity
Cogo Optronics	Juniper Networks	Tektronix
Comcast	KDDI R&D Laboratories	Tellabs
Cortina Systems	Kotura, Inc.	TeraXion
CyOptics	LeCroy	Texas Instruments
Dell, Inc.	LSI Corporation	Time Warner Cable
Department of Defense	Luxtera	TriQuint Semiconductor
Deutsche Telekom	M/A-COM Technology Solutions, Inc.	u^2t Photonics AG
ECI Telecom Ltd.	Marben Products	Verizon
Emcore	Maxim Integrated Products	Vitesse Semiconductor
Emulex	Mayo Clinic	Xilinx
Ericsson	Metaswitch	Xtera Communications
ETRI	Mitsubishi Electric Corporation	Yamaichi Electronics Ltd.
EXFO	Molex	ZTE Corporation