Implementation Agreement for Integrated Dual Polarization Intradyne Coherent Receivers

IA # OIF-DPC-RX-01.2

November 14, 2013

Implementation Agreement to be revised and approved
by the Optical Internetworking Forum
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Working Group: **Physical and Link Layer (PLL) Working Group**

TITLE: **Implementation Agreement for Intradyne Coherent Receivers**
IA # OIF-DPC-RX-01.2

SOURCE:

MAINTENANCE EDITOR

John E. Johnson, Ph.D.
Avago Technologies, Inc.
9999 Hamilton Blvd.
Breinigsville, PA 18031
Phone: +1-484-397-2368
Email: john.johnson@avagotech.com

WORKING GROUP CHAIR

David R. Stauffer, Ph.D.
IBM Corporation
1000 River Road, MC 862J
Essex Jct., VT 05452
Phone: +1-802-769-6914
Email: dstauffe@us.ibm.com

WORKING GROUP VICE CHAIR

Karl Gass
Sandia National Laboratories
P. O. Box 5800 MS-0874
Phone: +1-505-844-8849
Email: iamthedonutking@mac.com

ABSTRACT: This contribution reflects the results from the first maintenance cycle of IA# OIF-DPC-RX-01.1 Implementation Agreement for Intradyne Coherent Receivers.

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For additional information contact:
The Optical Internetworking Forum, 48377 Fremont Blvd.,
Suite 117, Fremont, CA 94538
510-492-4040 ✦ info@oiforum.com

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2 List of Figures

3 List of Tables

4 Document Revision History

Version	Date	Description
OIF-DPC-RX-01.0 Initial release	16 April 2010	Initial release
OIF-DPC-RX-01.1	20 Sept 2011	Various editorial corrections. Various additions to the descriptive text. Addition of table of operating characteristics to section 9 specifying several parameters. Addition of table of fiber characteristics to section 10 specifying several parameters. Update or addition of several mechanical dimensions of package including reduction of body length from 60mm to 50mm. Designation of DC pins 5&6 for connecting internal monitor photodiode. Removal of subscripts distinguishing PD bias pins to accommodate multiple versions already in use. Removal from appendix of items now specified in IA body.
OIF-DPC-RX-01.2	14 Nov 2013	Multiple editorial changes to refer to the original Integrated Intradyne Coherent Receiver form factor as “Type 1.” Multiple revisions to add the definition of a new “Gen-2” reduced size form factor as “Type 2.” Delete the 6V photodiode bias option in Table 4. Add an informative test method and nomenclature for the sign of I-Q phase as Figure 7. Delete Appendix C, FPC Interfaces (Informative)

5 Introduction

This document details an implementation agreement for an integrated intradyne coherent receiver initially targeting 100G PM-QPSK applications with nominal symbol rates up to 32 GBaud. While specifically addressing 100G PM-QPSK applications, this Implementation Agreement strives to remain modulation format and data rate agnostic whenever practical to maximize applicability to future market requirements. This document is not a multi-source agreement, but is expected to be the foundation of future MSAs.

100G DWDM represents a significant development expense for component and system suppliers. Currently available photonics components addressing the market are discrete and varied. A need for integration has been identified in order to meet cost and size objectives. This implementation agreement aims to reduce risk to component suppliers and users by identifying and specifying common features and properties of the devices that will enable them to broadly meet the needs of this emerging market.

This Implementation Agreement originates from the “100G long-distance DWDM integrated photonics” project, undertaken in the Physical Link Layer working group. This Implementation Agreement defines: (1) Required functionality. (2) High speed electrical interfaces. (3) Low speed electrical interfaces. (4) Mechanical requirements. (5) Environmental requirements. Also included are informative specifications for (6) opto-electronic interfaces. Two distinct electro-mechanical form factors are defined in this revision of the Implementation Agreement. This Implementation Agreement does not define the type of technology used in photonics sub-components, nor expected optical transmission performance of systems using receivers conforming to this Implementation Agreement. This Implementation Agreement is intentionally structured not to preclude differentiation of product or system performance.

6 Functionality

The required functionality for the integrated coherent receiver is shown within the dashed line in Figure 1. A single component containing the described functionality is not required to meet the objectives of this implementation agreement.

As indicated in Figure 1, the coherent receiver requires the following basic functionality:

1. Eight (8) photo-detectors, comprised of 4 sets of balanced detectors
2. Four (4) linear amplifiers with differential output
3. Two (2) ninety degree hybrid mixers with differential outputs
4. A polarization splitting element, separating the input signal into two orthogonal polarizations, with each polarization delivered to a hybrid mixer
5. A polarization maintaining power splitter or polarization splitting element, splitting the local oscillator power equally to the two hybrid mixers.
6. An optical power tap and monitor photodiode in the signal input path.
7. A variable optical attenuator in the signal input path between the signal power tap and the signal polarization splitting element.

At a minimum, the first 3 of the above functions must be contained in a single photonics component to meet the objectives of this implementation agreement for the Type 1 form factor integrated coherent receiver. The first 5 of the above functions must be contained in a single photonics component to meet the objectives for the Type 2 form factor integrated coherent receiver. The remaining features are optional in both cases.

The polarization channels are indicated in Figure 1 as ‘X-Pol’ and ‘Y-Pol’ and the phase channels for each labeled XI, XQ and YI,YQ respectively. The complementary outputs for each channel are labeled ‘p’ and ‘n’. X and Y indicate a pair of mutually orthogonal polarizations of any orientation. I and Q are mutually orthogonal phase channels in each polarization. I and Q are established relative to the phase of the Local Oscillator where the relationship of the phase of the Signal in the Q channel to the Local Oscillator is either advanced or delayed by nominally 90 degrees as compared to the relationship in the I channel. The relative advance or delay of the Q channel in the Y polarization channel should correspond to that in the X polarization channel. The testing method and nomenclature of Figure 7 in Appendix B shall be used to establish the relative advance or delay of the Q channel with respect to the I channel. Outputs ‘p’ and ‘n’ are the complementary outputs for each polarization-phase channel and are such that the output voltage for ‘p’ increases as the Signal and Local Oscillator approach the in-phase condition to form constructive interference, and the output voltage for ‘n’ decreases under the same conditions.

Additional required functionality for the integrated coherent receiver includes:

- Automatic Gain Control (AGC) and/or Manual Gain Control (MGC)
- User settable output voltage swing
- Independent output swing adjustment for each of the four outputs
- Peak indicators for each output

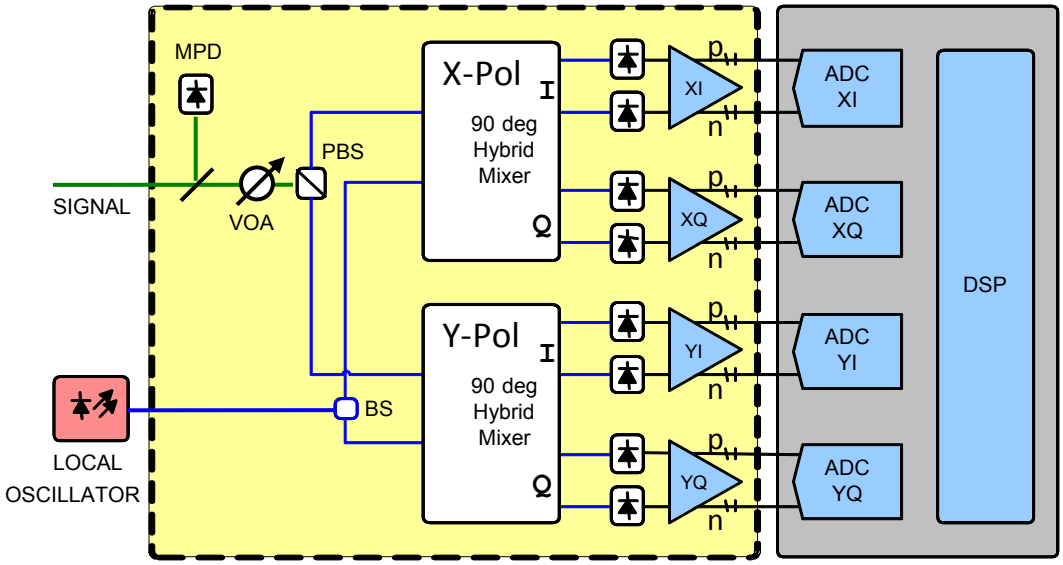


Figure 1: Functional diagram of a dual polarization intradyne coherent receiver. The yellow area enclosed by the dashed line indicates the functionality specified in this implementation agreement.

7 High Speed Electrical Interface

The high speed electrical interface is co-planar waveguide, consistent with the pitch and pin definition detailed in Table 1, Table 2, and Figure 2.1 and 2.2. It is noted for the channel pin-out shown in Figure 2.1 and 2.2 that X, Y, I, Q, p, and n are consistent with the descriptions in Section 6. It is also noted that alternate polarities for the differential signals specified in Figure 2.1 and 2.2 are acceptable.

Table 1: High-speed electrical interface description.

Parameter	Form Factor	Value	Notes
Interface Type	All	Differential	
Channel Number	All	4	
Channel Configuration	Type 1 Type 2	G-S-G-S-G G-S-S-G	Per Figure 2.1 Per Figure 2.2
Signal Line Coupling	All	AC	
Signal Line Impedance	Type 1 Type 2	50 ohm to Ground 100 ohm Differential	
Channel Pin-out	All	XI XQ YI YQ	Per Figure 2.1 and Figure 2.2
Differential Pin-Out	All	Signal Complimentary Signal	p n

Table 2: High-speed electrical interface dimensions.

Parameter	Symbol	Form Factor	Min	Typ	Max	Units
Lead Pitch	A	All		1.0		mm
Lead Length (referenced from outside wall of package, as defined by dimension LP2 in Section 10)	B	Type 1 Type 2	2.00 1.50		3.00	mm
Signal Lead Width	C	All	0.10		0.30	mm
Ground Lead Width	D	All	0.10		0.50	mm
Channel Pitch	E	Type 1 Type 2		5.0 3.0		mm
Signal to Complimentary Signal Pitch	F	Type 1 Type 2		2.0 1.0		mm

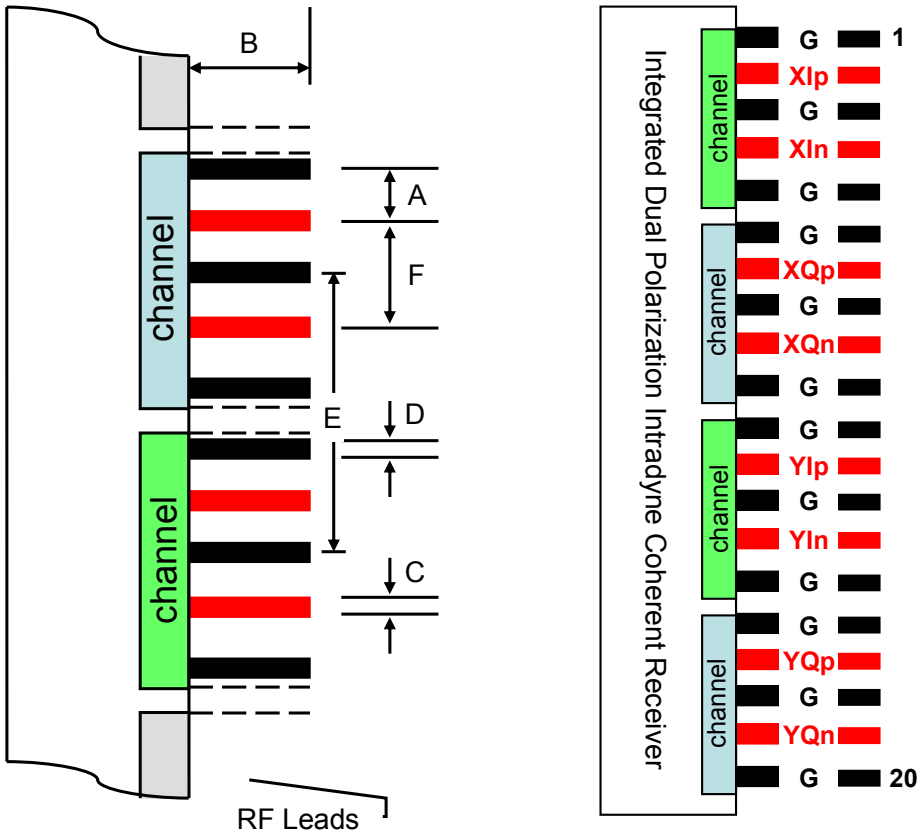


Figure 2.1: High-speed electrical interface definition for Type 1 form factor.

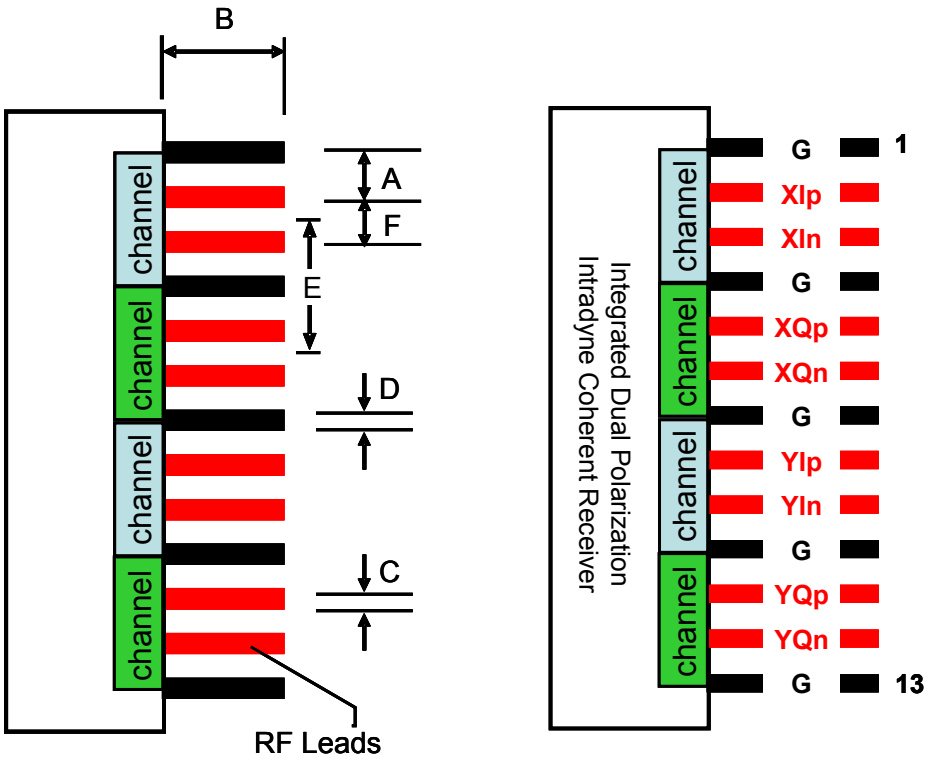


Figure 2.2: High-speed electrical interface definition for Type 2 form factor.

8 Low Speed Electrical Interface

The low speed electrical connections for the Type 1 form factor are provided through 40 pins, located and numbered as shown in Figure 3.1. The low speed electrical connections for the Type 2 form factor are provided through 34 pins, located and numbered as shown in Figure 3.2. Unused pins are not required to be present.

The photocurrent of each photodiode, or a representative equivalent quantity, shall be measurable.

The pin pitch is specified to be 1.27 mm for Type 1 and 1.0 mm for Type 2 form factor.

The pin definitions for the low speed electrical interfaces are provided in Tables 3.1 and 3.2.

Table 3.1: Low speed electrical interface pin definition for Type 1 form factor.

Pin #	Symbol	Description		Pin #	Symbol	Description
1	SD-Y	Shutdown YI (optional)		40	RFU	Reserved for Future Use
2	PI-YI	Peak Indicator YI		39	PI-XQ	Peak Indicator XQ
3	GA-YI	Gain Adjust YI		38	GA-XQ	Gain Adjust XQ
4	OA-YI	Output Amplitude Adjust YI		37	OA-XQ	Output Amplitude Adjust XQ
5	MPD+	Monitor Photodiode Cathode (optional)		36	RFU	Reserved for Future Use
6	MPD-	Monitor Photodiode Anode (optional)		35	MC/AGC-X	MGC/AGC Selection X (optional)
7	VCC-YI	Supply Voltage Amplifier YI		34	VCC-XQ	Supply Voltage Amplifier XQ
8	GND	Ground Reference		33	GND	Ground Reference
9	PD-YI	Photodiode Bias Voltage YI[1]		32	PD-XQ	Photodiode Bias Voltage XQ[1]
10	PD-YI	Photodiode Bias Voltage YI[1]		31	PD-XQ	Photodiode Bias Voltage XQ[1]
11	PD-YQ	Photodiode Bias Voltage YQ[1]		30	PD-XI	Photodiode Bias Voltage XI[1]
12	PD-YQ	Photodiode Bias Voltage YQ[1]		29	PD-XI	Photodiode Bias Voltage XI[1]
13	GND	Ground Reference		28	GND	Ground Reference
14	VCC-YQ	Supply Voltage Amplifier YQ		27	VCC-XI	Supply Voltage Amplifier XI
15	MC/AGC-Y	MGC/AGC Selection Y (optional)		26	RFU	Reserved for Future Use
16	RFU	Reserved for Future Use		25	RFU	Reserved for Future Use
17	OA-YQ	Output Amplitude Adjust YQ		24	OA-XI	Output Amplitude Adjust XI
18	GA-YQ	Gain Adjust YQ		23	GA-XI	Gain Adjust XI
19	PI-YQ	Peak Indicator YQ		22	PI-XI	Peak Indicator XI
20	RFU	Reserved for Future Use		21	SD-X	Shutdown XI (optional)

[1]PD-YI, PD-YQ, PD-XI, PD-XQ each represent 2 pins wherein each one of the two pins independently supplies the bias voltage to correspondingly each one of the two photodiodes for the labeled Polarization / Phase channel.

Table 3.2: Low speed electrical interface pin definition for Type 2 form factor.

Pin #	Symbol	Description		Pin #	Symbol	Description
1	RFU	Reserved for Future Use		34	RFU	Reserved for Future Use
2	RFU	Reserved for Future Use		33	RFU	Reserved for Future Use
3	MC/AGC	MGC/AGC Selection (optional)		32	SD	Shutdown (optional)
4	MPD+	Monitor Photodiode Cathode (optional)		31	VOA1	VOA1 Adjust Voltage (optional)[2]
5	MPD-	Monitor Photodiode Anode (optional)		30	VOA2	VOA2 Adjust Voltage (optional)[2]
6	PD-YI	Photodiode Bias Voltage YI[1]		29	PD-XQ	Photodiode Bias Voltage XQ[1]
7	PD-YI	Photodiode Bias Voltage YI[1]		28	PD-XQ	Photodiode Bias Voltage XQ[1]
8	PD-YQ	Photodiode Bias Voltage YQ[1]		27	PD-XI	Photodiode Bias Voltage XI[1]
9	PD-YQ	Photodiode Bias Voltage YQ[1]		26	PD-XI	Photodiode Bias Voltage XI[1]
10	PI-YI	Peak Indicator YI		25	PI-XQ	Peak Indicator XQ
11	GA-YI	Gain Adjust YI		24	GA-XQ	Gain Adjust XQ
12	OA-YI	Output Amplitude Adjust YI		23	OA-XQ	Output Amplitude Adjust XQ
13	VCC-Y	Supply Voltage Amplifier Y		22	VCC-X	Supply Voltage Amplifier X
14	GND	Ground Reference		21	GND	Ground Reference
15	OA-YQ	Output Amplitude Adjust YQ		20	OA-XI	Output Amplitude Adjust XI
16	GA-YQ	Gain Adjust YQ		19	GA-XI	Gain Adjust XI
17	PI-YQ	Peak Indicator YQ		18	PI-XI	Peak Indicator XI

[1] PD-YI, PD-YQ, PD-XI, PD-XQ each represent 2 pins wherein each one of the two pins independently supplies the bias voltage to correspondingly each one of the two photodiodes for the labeled Polarization / Phase channel.
[2] Pins 31 and 30 (VOA1 and VOA2) shall not be connected internally to Ground.

9 Environmental and Operating Characteristics

Basic operating characteristics are listed in Table 4.

Table 4: Operating Characteristics

Parameter		Unit	Min	Typ	Max	Note
Symbol Rate		GBaud		32		
Operating Frequency	C-Band	THz	191.35		196.20	#1
	L-Band		186.00		191.50	
Amplifier Supply Voltage		V		3.3		
Photodiode Bias Voltage	Option 3.3	V	3.135	3.3	3.465	#2
	Option 5.0		4.75	5.0	5.25	
Monitor Photodiode Bias Voltage	Option 3.3	V	3.135	3.3	3.465	
	Option 5.0		4.75	5.0	5.25	
Operating Temperature	Standard	°C	-5		75	#3
	Preferred		-5		80	
Operating Humidity		%RH	5		85	#4

#1 Minimum supported range. On 50 GHz grid, as defined in G694.1. At least one of the two frequency bands to be supported.
#2 Vendor to state which Bias Voltage option or options are allowed both for signal Photodiodes and Monitor Photodiodes.
#3 Max temperature is the outside surface temperature of the photonic module and is to be measured in the “hot zone” of the case.
#4 Non condensing.

10 Mechanical

The mechanical requirements for the integrated coherent receiver are detailed in Figures 3.1, 3.2, 4.1 and 4.2, and Tables 5 and 6. The requirements include:

- Fiber input and high speed electrical output located on opposite sides
- Signal input fiber to be Single Mode Fiber (SMF)
- Local oscillator fiber to be Polarization Maintaining Single Mode Fiber (PM SMF)
- DC supply and control voltages applied from remaining sides
- The thermal transfer path shall be through the PCB side of the device
- The devices hot region shall be within the area indicated in Figures 3.1 and 3.2.
- Use of appropriate strain relief in high speed electrical pins

For Type 1 form factor implementations with BS and/or PBS functions located external to the main photonics component, the maximum envelope shall pertain only to the main photonics component.

Table 5: Fiber Characteristics

Parameter		Unit	Min	Typ	Max	Note
Minimum Fiber Bend Radius: SM-PMF on Local Oscillator Input	Standard	mm			20	#1 #2 #3
	Preferred				15	
Minimum Fiber Bend Radius: SMF on Signal Input		mm			15	

#1 The polarization state in any PM fiber shall be aligned to the slow axis of the PM fiber.
#2 The slow axis of any PM fibers shall be aligned to the connector key.
#3 All fibers to be uniquely identified.

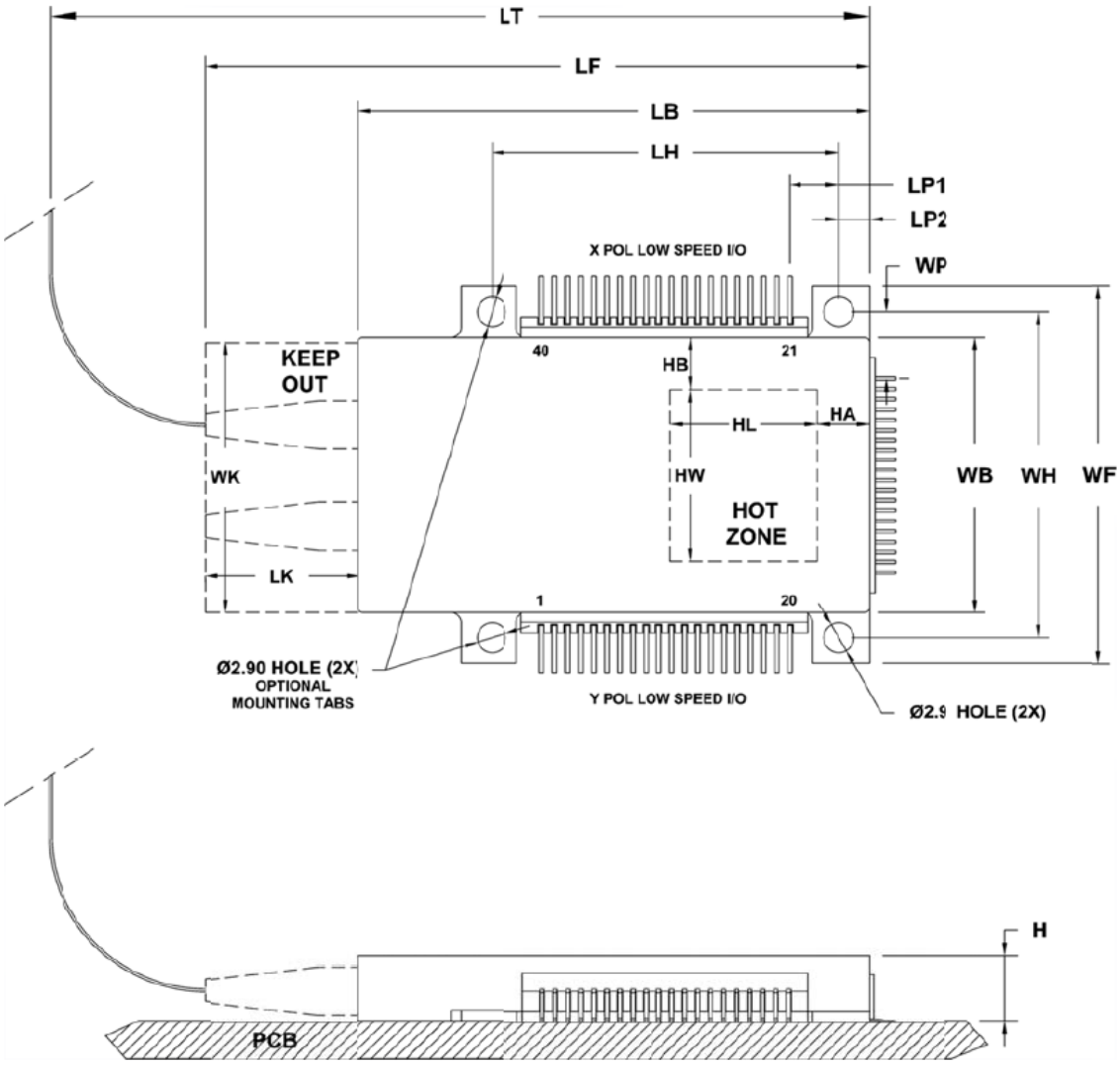


Figure 3.1: Mechanical diagram for Type 1 form factor.

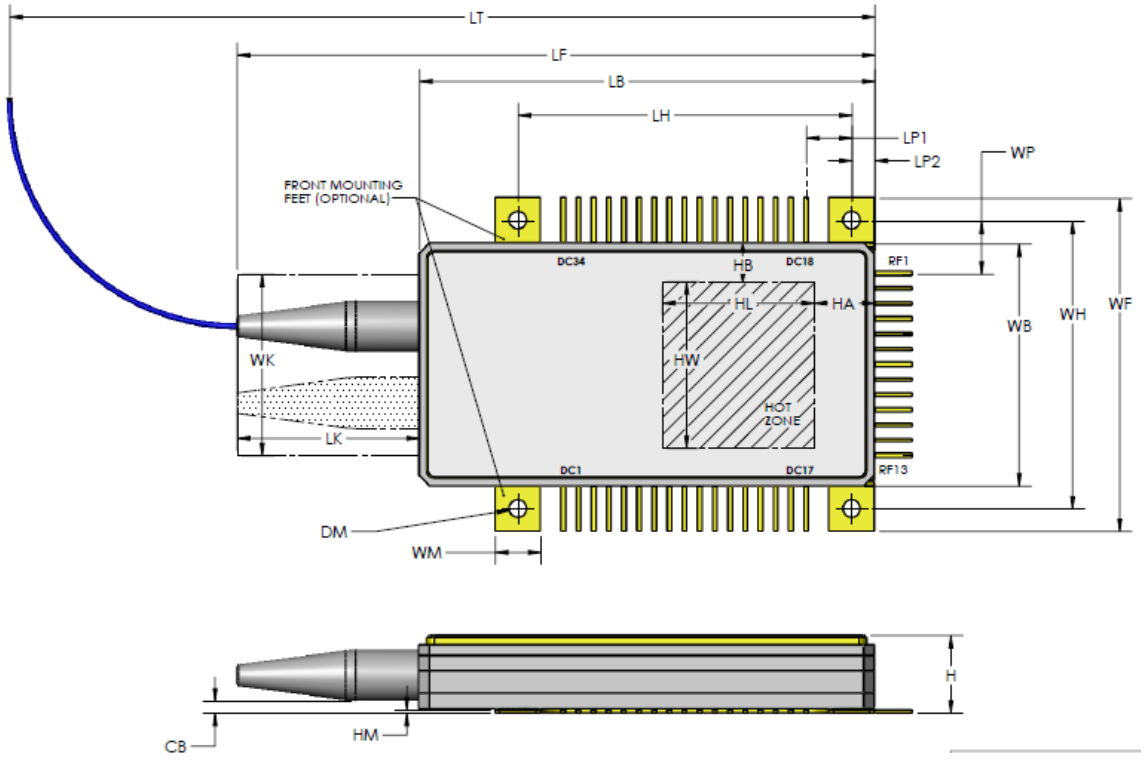


Figure 3.2: Mechanical diagram for Type 2 form factor.

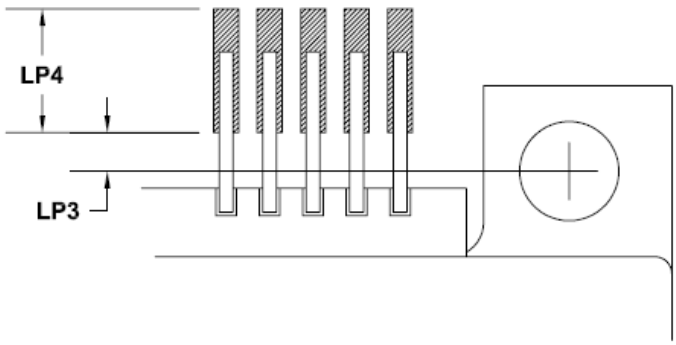


Figure 4.1: DC/control pin landing pad location for Type 1 form factor.

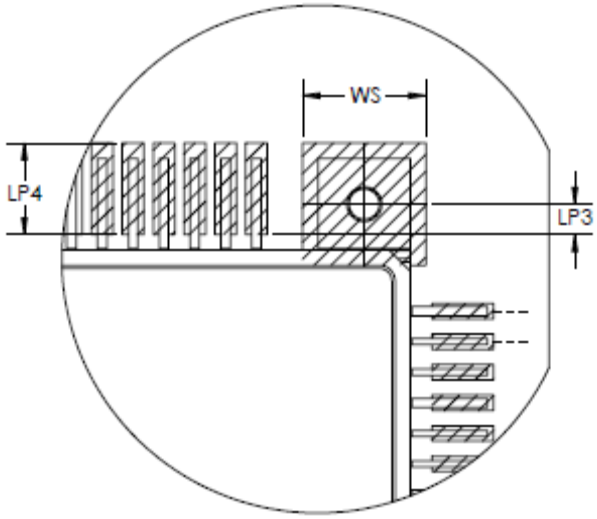


Figure 4.2: Mounting flange and DC/control pin landing pad location for Type 2 form factor.

Table 6: Mechanical dimensions. All dimensions in mm.

Symbol	Description	Type 1 Form Factor			Type 2 Form Factor			Note
		Min	Nom	Max	Min	Nom	Max	
H	Package height			9	3.5		6.5	
LT	Total length, including 90 degree fiber bend			90			60	
LF	Full length of package, including fiber boots			70			45	
LB	Length of package body			50			33	
LH	Distance between mounting holes (optional)		34			22		
LP1	Distance between mounting hole center and center of last dc pin		4.935			3.0		
LP2	Distance between mounting hole center and RF end of package		3			1.5		
LP3	DC/Control pin landing pad location relative to mounting hole center			1.5		1.0		Note #2
LP4	DC/Control pin landing pad length	2.5				3.0		
WF	Width of package, including mounting flanges and DC pins			41			22	
WH	Distance between mounting holes		32			19		
WB	Width of package body		27			16	17	
WP	Distance between mounting hole center and first RF pin center		6.5			3.5		
HA	Location of hot region relative to package edge	3		4	3		4	
HB	Location of hot region relative to package edge	HW to be centered in package			HW to be centered in package			
HW	Width of hot region			WB			WB	Centered in package
HL	Length of hot region			25			20	
WK	Width of boot area Keep-Out region			22			12	Centered to Package
LK	Length of boot area Keep-Out region	(Max LF) - LB			(Max LF) - LB			Maximum
WM	Width of mounting flanges				2.5	3	4	
HM	Height of mounting flanges					0.2	0.4	Note #1
CB	Clearance under fiber boots				0.3			
DM	Diameter of mounting holes		2.9		1.55	1.60	1.65	
WS	Width of mounting foot pad					3.5		

#1 Type 1 mounting flanges are screw-down type. Type 2 mounting flanges are screw-down and/or solder type.
#2. For Type 1 form factor LP3 is offset away from the package body. For Type 2 form factor LP3 is offset towards the package body. Refer to Figures 4.1 and 4.2.

11 References

11.1 Normative references
11.2 Informative references

12 Appendix A: Glossary

ADC	Analog to Digital Converter
AGC	Automatic Gain Control
BS	Beam Splitter
CMRR	Common Mode Rejection Ratio
DSP	Digital Signal Processor
GBaud	10^9 Symbols per second
IA	Implementation Agreement
LO	Local Oscillator
MGC	Manual Gain Control
MPD	Monitor Photodiode
MSA	Multi-Source Agreement
OIF	Optical Internetworking Forum
PBS	Polarization Beam Splitter
PCB	Printed Circuit Board
PM-QPSK	Polarization Multiplexed Quadrature Phase Shift Keying
THD	Total Harmonic Distortion
VOA	Variable Optical Attenuator

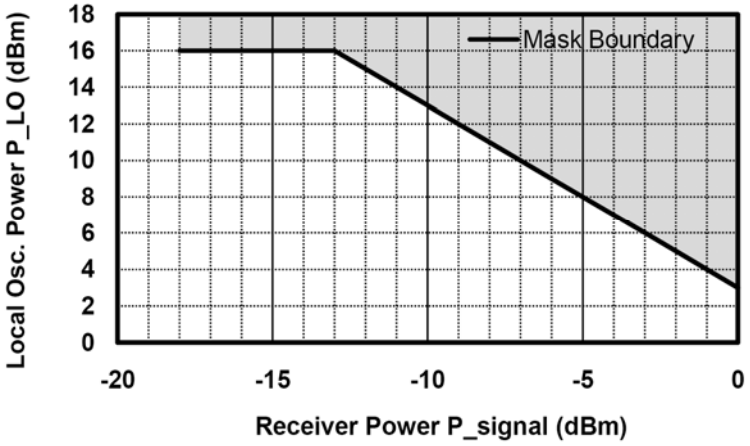
13 Appendix B: Opto-Electrical Properties (informative)

Opto-electrical properties consistent with the application and objectives described in the 100G framework document are provided in Table 7. These values are to be interpreted as target values. It is expected that values will be updated as necessary and become normative and moved to the main body of this document as the technology matures.

Table 7: Opto-electrical properties

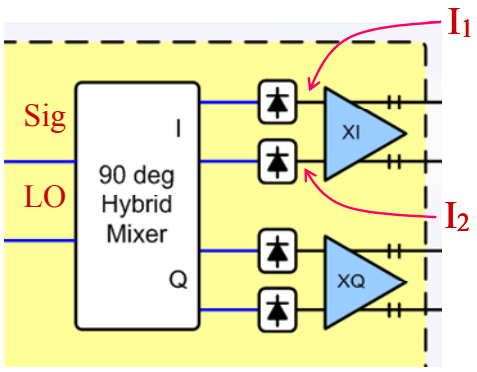
Parameter	Units	Min	Typ	Max	Comments
Symbol Rate	GBaud			32	
Operating Signal Power	dBm	-18	-10	0	Average optical power
Local Oscillator Power	dBm				See Figure 5 for recommended operating conditions.
Linear output swing adjustment range Standard Extended	 mVppd mVppd	 300 400	 500	 700 900	Peak to peak, differential, AC coupled
Maximum Gain Control Bandwidth	MHz		5		Settable via external control. Measured by applying step at gain control node such that output changes 5%. BW is estimated by 0.22/Tr where Tr is 20-80% rise/fall of the output envelope step.
Total Harmonic Distortion (THD) DC current = 1.3 mA AC = 0.36mApp in to each PD $V_{OUT\|DIFF}$ = 500mVpp F_{IN} = 1GHz ± 10%	%			5	Assumptions: P(SIG) = -10dBm P(LO) = 13dBm Excess loss = 2dB, PD Responsivity = 0.8A/W
Common Mode Rejection Ratio ($CMRR_{DC}$) Signal to I & Q LO to I & Q	 dBe dBe			 -20 -12	See Figure 6 for definition
Common Mode Rejection Ratio ($CMRR_{22GHz}$) Signal to I & Q LO to I & Q	 dBe dBe			 -16 -10	See Figure 6 for definition

Small Signal Bandwidth (3dB)	GHz		22		
Low Frequency Cutoff	kHz			100	AC coupling
Phase Error	±deg			5	Between XI and XQ and between YI and YQ See Figure 7 for test method and nomenclature.
Optical Reflectance	dB			-27	Signal and LO ports. Per ITU-T G.959.1
Output Electrical Return Loss (S22): f < 16 GHz 16 GHz < f < 24 GHz 24 GHz < f < 32 GHz	 dB dB dB	 10 8 6			
Skew: p, n	ps			2	
Channel skew	ps			10	Time difference between earliest and latest channel. Includes channel skew variation.
Channel skew variation	ps			5	Temporal variation in the skew between any 2 channels due to case temperature, wavelength, input optical power, amplifier gain, and aging. Time for channel defined as mean of p and n.
Signal MPD responsivity	A/W		0.05		Optional feature
Signal MPD to LO input optical isolation	dB		45		Optional feature
VOA Type		Normally Open			Optional feature
VOA control voltage	V			9	Optional feature
VOA attenuation range	dB	10			Optional feature



P_signal (dBm)	P_LO (dBm)	I_diff_pp (mA)
0	3	0.715
-3	6	0.715
-6	9	0.715
-10	13	0.715
-13	16	0.715
-16	16	0.506
-18	16	0.402

Figure 5: Recommended maximum allowable local oscillator power mask as a function of signal power to the integrated receiver for linear operation. A photodiode responsivity of 0.8A/W, NRZ coding, back to back operation, 0.715mA peak to peak differential linear input dynamic range, and an excess loss of 2dB are assumed . P_LO power level is as applied prior to the splitter equally dividing LO between X and Y partitions.



$$\text{CMRR (electrical)} = 20\log[|I_1-I_2|/(I_1+I_2)]$$

Figure 6: CMRR definition.

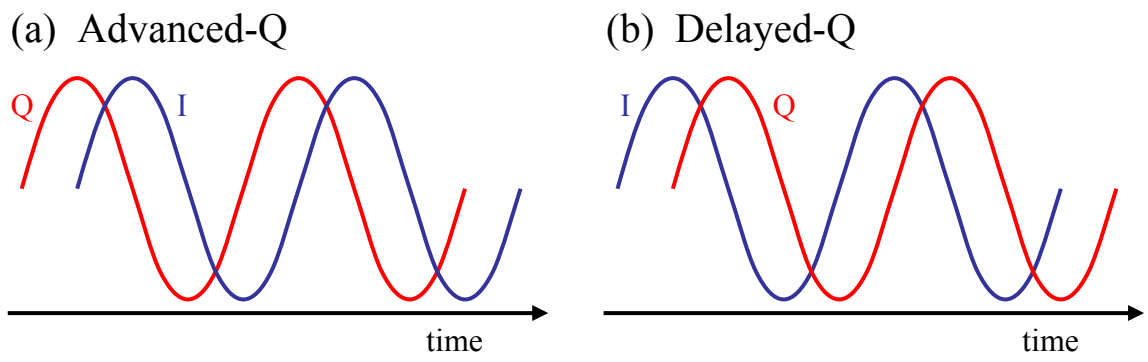


Figure 7: Test method and nomenclature for the sign of I-Q phase. The measurement shall be made by the heterodyne technique with the frequency of the Signal input greater than the frequency of the LO input and the I and Q channel electrical outputs measured in the time domain. The relative phase shown in (a) shall be referred to as "Advanced-Q" and the relative phase shown in (b) shall be referred to as "Delayed-Q" for the case where 'p' and 'n' RF outputs have the same relative order for both I and Q.

14 Appendix C: Open Issues / current work items

15 Appendix D: List of companies belonging to OIF when document is approved

Acacia Communications
ADVA Optical Networking
Agilent Technologies
Alcatel-Lucent
Altera
AMCC
Amphenol Corp.
Anritsu
Applied Communication Sciences
AT&T
Avago Technologies Inc.
Broadcom
Brocade
Centellax, Inc.
China Telecom
Ciena Corporation
Cisco Systems
ClariPhy Communications
Coriant
Cortina Systems
CPqD
Department of Defense
Deutsche Telekom
Emcore
Ericsson
FCI USA LLC
Fiberhome Technologies Group
Finisar Corporation
Fujitsu
Furukawa Electric Japan
Google
Hewlett Packard
Hitachi
Hittite Microwave Corp
Huawei Technologies
IBM Corporation
Infinera
Inphi
Intel
JDSU
Juniper Networks
Kaiam
Kandou
KDDI R&D Laboratories
LeCroy
LSI Corporation
Luxtera
M/A-COM Technology Solutions, Inc.
Marben Products
Metaswitch
Mindspeed
Mitsubishi Electric Corporation
Molex
MoSys, Inc.
MultiPhy Ltd
NEC
NeoPhotonics
NTT Corporation
Oclaro
Optelian
Orange
PETRA
PMC Sierra
QLogic Corporation
Ranovus
Semtech
Skorpios Technologies
Sumitomo Electric Industries
Sumitomo Osaka Cement
TE Connectivity
Tektronix
Tellabs
TELUS Communications, Inc.
TeraXion
Texas Instruments
Time Warner Cable
TriQuint Semiconductor
u2t Photonics AG
US Conec
Verizon
Xilinx
Xtera Communications
Yamaichi Electronics Ltd.