Working Group: **Physical and Link Layer (PLL)**

TITLE: **Very Short Reach Interface Level 5 (VSR-5): SONET/SDH OC-768 interface for Very Short Reach (VSR) applications.**

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Abstract: Implementation Agreement for an optical interface capable of nominal 40 Gbit/s aggregate bit rate intra-office systems for link distances up to 2 km.

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4 DOCUMENT REVISION HISTORY

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5 INTRODUCTION

This technical document specifies a set of functional SONET/SDH OC-768/STM-256 interfaces for Very Short Reach (VSR) applications hereafter known as VSR-5. The complete solution set is intended to address the set of reference applications, while minimizing overall network and operational cost and complexity.

The goals for the individual solutions are:

- Broad market potential
- Broad use in the context of the reference applications listed (most customers)
- Broad supplier support (most suppliers)
- Compatible (Suitable for an SFI-5 electrical interface carrying SONET framed data. A VSR link can be part of a SONET/SDH network and not cause problems in the SONET/SDH network.)
- Distinct from other solutions in end-user cost or application space (Cost to include fiber connections.)
- Technically feasible
- Economically feasible
- 2x cost for 4x speed, exponentially dropping (compared with OC-192 VSR) Solutions must use a field-terminable cable

The objectives for the whole solution set:

- Must minimize overall network and operational cost and complexity.
- The set should contain the minimum number of solutions required to address the reference applications, while meeting the other Objectives stated herein.
- Must include a single-mode (G.652), single-fiber, serial solution.
- Timeframe for general availability of at least one solution should be H1'02. Timeframe for cost optimization is early volume deployment.

6 INTERFACE DESCRIPTION

This section provides a brief introduction of the VSR-5 interface. Section 7 contains a 12 channel parallel optics solution. Section 8 describes an SMF 4x10 CWDM solution. Section 9 describes a serial SMF solution.

The application of the OC-768 VSR interface is to interconnect co-located equipment. Due to the short distances, an alternative that is less costly than current OC-768 short reach solutions is desired. Examples of equipment that is often co-located and interconnected within a central office (CO) include:

1. Routers
2. Dense Wavelength Division Multiplexers (DWDM) terminals
3. SONET/SDH Add-drop multiplexers (ADMs), and Crossconnects.

The VSR-5 interfaces described in sections 7 and 8 will be able to inter-work with OTN and SDH networks by the application of a clock filter function ensuring jitter requirements of ITU-T G.783 for SONET/SDH and G.8251 for G.709 are met.

Shown in Figure 6.1 through Figure 6.5 below are the reference application models supported by VSR-5. Reference application 1 is a direct intra-office connection of up to 100 meters with no patch panels or junction boxes. Reference application 2 is an intra-office connection of up to 300m with zero to two patch panels. Reference application 3 is an inter-office connection of up to 600m with zero to two patch panels. Reference application 4 is an inter-office connection of up to 2000m with zero to four patch panels and two splices. Reference application 5 is an intra-office connection of up to 600m with zero to four patch panels and one photonic cross connect.

Figure 6.1: Reference application 1, intra-office, direct connection, 2m to 100m, no patch panels.

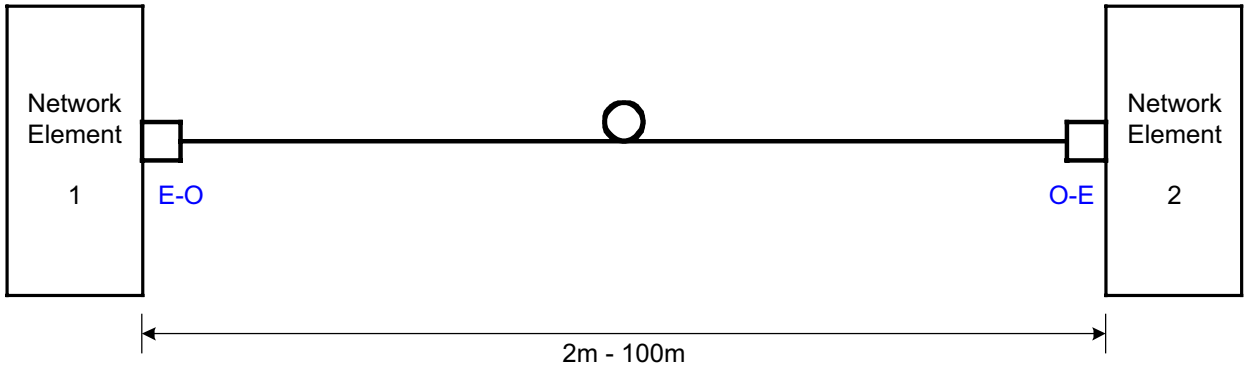


Figure 6.2: Reference application 2, intra-office, no PXC, 2m to 300m, with 0-2 patch panels.

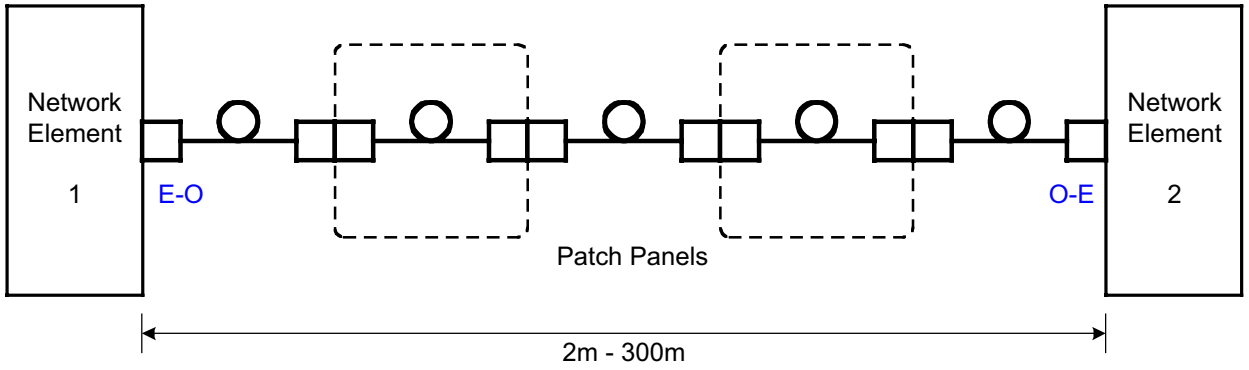


Figure 6.3: Reference application 3, inter-office, no PXC, 2m to 600m, with 0-2 patch panels.

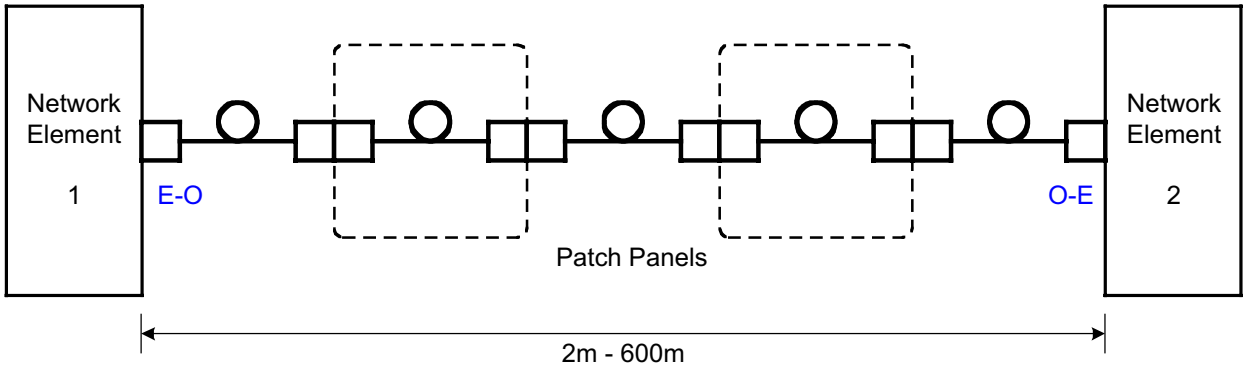


Figure 6.4: Reference application 4, inter-office, no PXC, 2m to 2km, with 0-4 patch panels and 0-2 splices.

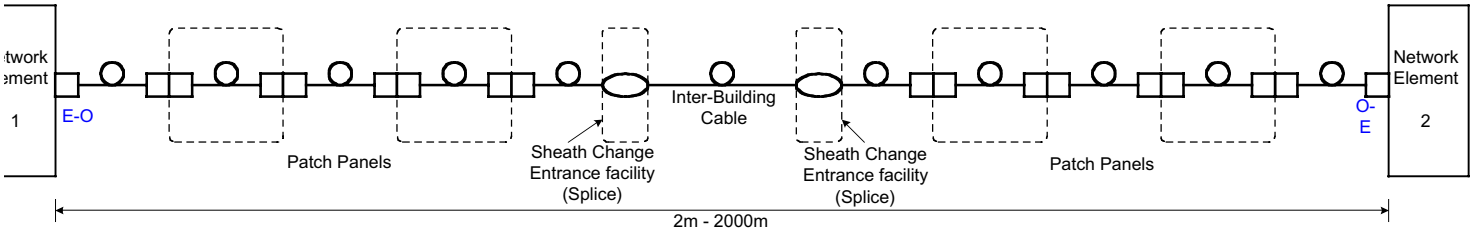


Figure 6.5: Reference application 5, intra-office, one PXC, 2m to 600m, with 0-4 patch panels.

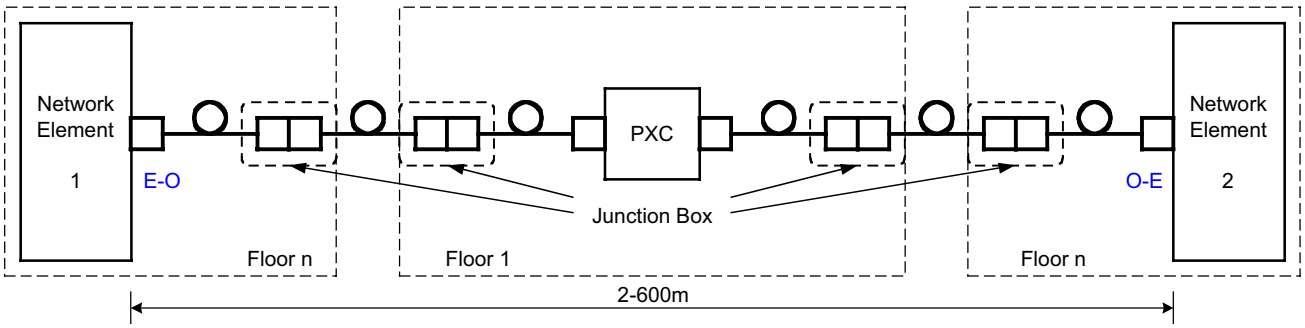


Table 6.1: Table relating reference applications to possible solutions.

Reference Model	Link description	12 x 3.3	4 x 10	Serial
1	2m to 100m intra-office direct connection, no patch panel or junction boxes	X	X	X
2	2m to 300m intra-office inter-connection, with 0-2 patch panels	X	X	X
3	2m to 600m intra-office inter-connection, with 0-2 patch panels		X	X
4	2m to 2km inter-office inter-connection, with 0-4 patch panels and 0-2 splices		X	X
5	2m to 600m intra-office inter-connection with exactly one PXC in the interconnect, and 0-4 junction boxes			X

The scope of VSR-5 includes normative specifications and also informative elements.

Specifications pertaining to the interface between Network Elements, as depicted in Figures 6.1 through 6.5, are **normative**. Examples include (a) the physical layer signaling (temporal and spectral) parameters of signals traveling between Network Elements, and (b) the ordering and format of digital information traveling between network elements.

Specifications pertaining to interfaces within Network Elements are **informative**. Examples include the ordering and format of information traversing the SFI-5 interface that is assumed to be, but not required to be, within Network Elements.

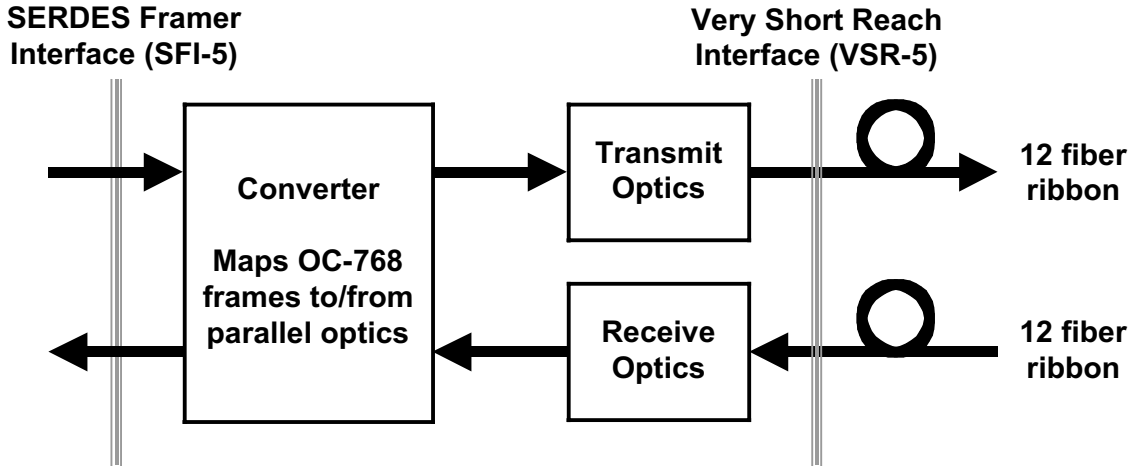
7 TWELVE CHANNEL PARALLEL OPTICS

This OC-768 Very Short Reach (VSR) interface utilizes parallel optic technology with a twelve-channel array of 850nm Vertical Cavity Surface Emitting Lasers (VCSELs). It addresses reference applications 1 and 2. The target performance of the VSR interface is to provide a link for a SONET/SDH OC-768 scrambled data stream over standard 50/125 μm-core, 400 or 500 MHz.km multimode ribbon fiber at distances up to 100 meters. 50/125 μm-core, 2000 MHz.km high bandwidth multimode fiber is supported at distances of 300 meters.

This document defines the parallel optical interfaces required for a link operating over multimode fiber.

The OC-768 VSR interface is a bi-directional interface. A functional block diagram is illustrated in Figure 7.1.

Figure 7.1 Block diagram of 12 channel interface.



The transmit direction includes a Converter, laser driver, and 850nm VCSEL array, whose output is coupled to a multimode fiber cable plant, supporting a distance up to 300 meters. The Converter receives signals from a 16 bit wide data bus at 2.488 Gb/s per channel from an external OC-768 Framer utilizing the SFI-5 electrical interface. The 16 bit parallel bus is mapped onto 12 parallel channels. The twelve channels are forwarded to the parallel optic transmitter, which converts the electrical signal to an optical signal and transmits the data along the twelve optical fibers in the ribbon fiber at a bit rate of 3.318 Gb/s per channel.

The parallel optical interface receives the twelve optical signals from the fiber ribbon cable at a data rate of 3.318 Gb/s. The parallel optics receiver converts

the signal to an electrical equivalent. This signal is recombined to a 16 bit wide data stream in the Converter for connection to the OC-768 framer chip.

The SERDES Framer Interface for OC-768 (SFI-5) shown in the block diagram in Figure 7.1 is compliant with the OIF SFI-5 Implementation Agreement (IA) [2] (at SERDES interface) but limited to SONET/SDH framed data at the nominal lane rate of 2.488 Gb/s (G.707). The parallel optical interface (OC-768 VSR-5) is described in detail in Section 7.2.

7.1 Converter

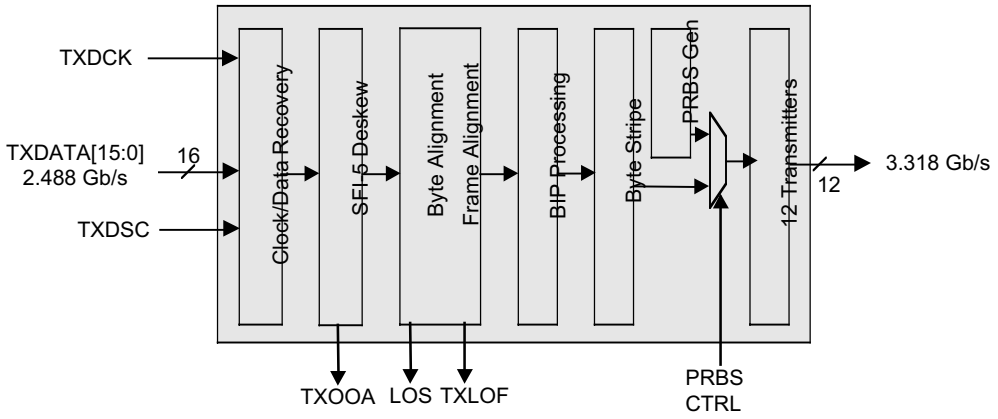
7.1.1 General Description

The Converter performs the general function of mapping an SFI-5 datastream to 12 channels for output to parallel transmit optics in the transmit direction. It also performs the reverse function of receiving 12 channels of data from a parallel optical receiver and mapping the data into an SFI-5 datastream in the receive direction. In order to perform these functions the Converter contains all the digital circuitry necessary for deskewing data in both directions, frame and byte alignment, state machine logic as well as the analog circuitry required for clock and data recovery and clock generation for all internal and external requirements and for all signal inputs and outputs. Also included is an Internal Register Block (IRB), accessible through a two-wire interface, which is used to implement test requirements for the SFI-5 and optics interfaces as well as various performance monitoring and counting functions. The basic function of the Converter in the VSR link is shown in the functional block diagram of Figure 7.1.

7.1.2 Transmitter Block

The transmitter section of the Converter processes data in the transmit direction, from system to optics. It receives data in SFI-5 format at 2.488 Gb/s per channel, deskews the data channels, byte aligns and frames on the data, then byte stripes and outputs the data on 12 channels operating at 3.318 Gb/s. These functions are outlined in Figure 7.2.

Figure 7.2: Transmitter Functional Blocks



7.1.2.1 Data Recovery and SFI-5 Deskew

The transmitter recovers data independently on TXDATA[15:0] and TXDSC at 2.488 Gb/s per channel as described in the SFI-5 Implementation Agreement [2]. Although SFI-5 specifies that terminating devices must operate at data rates from 2.488 Gb/s to 2.7725 Gb/s, the VSR Converter is only required to accommodate a 2.488 Gb/s rate on its SFI-5 interface.

Data recovered on TXDATA[15:0] have up to the maximum amount of relative skew between them as is allowed by the SxI-5 Implementation Agreement [1]. Data on the latest channel may lag data on the earliest channel by up to the specified number of UI. Bit lane deskew is accomplished with the TXDSC channel. TXDSC is a reference channel containing replicated data from each of the 16 data channels in a frame format described in the SFI-5 Implementation Agreement (IA). The SFI-5 Interface and Deskew blocks contain the buffers, deskew controllers and delay elements necessary for lane-to-lane data deskewing. By comparing the data on each channel with its corresponding data on TXDSC, the skew between data and reference channel is deduced. Once the delay is known the delay element associated with that channel is adjusted for alignment between the data and reference channel. This is carried out on each channel successively until all data channels are deskewed relative to the reference channel and therefore relative to each other.

An out-of-alignment alarm TXOOA is set if pattern matching cannot be achieved on all 16 channels, and is cleared when it is achieved. After successfully deskewing the 16 channels, the skew on each channel is continuously monitored, allowing the Converter to track skew changes of up to the maximum amount allowed in the SFI-5 IA without introducing errors. A set of counters in the IRB is allocated for counting the instances of pattern mismatch between each

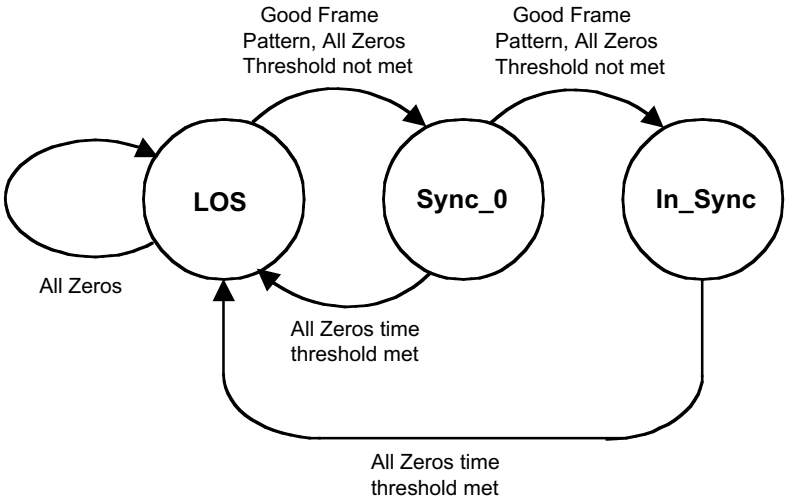
channel's data and the corresponding data on the deskew channel. The SFI-5 IA contains greater detail on the deskewing algorithm and TXDSC frame format.

7.1.2.2 Frame and Byte Align

Byte alignment and SONET framing information are obtained by examining the A1 and A2 bytes in the incoming data. Byte alignment is accomplished by locating a succession of A1 bytes in the data stream, and framing information is obtained by locating a number of A1 and A2 bytes around the A1/A2 boundary. It is recommended to use multiple A1's and A2's for this purpose. Data arriving at the Converter on the SFI-5 interface is in general not byte aligned on the SFI-5 bits 0 through 15, therefore no relationship should be assumed between the octets of the SONET frame and the SFI-5 bit lanes.

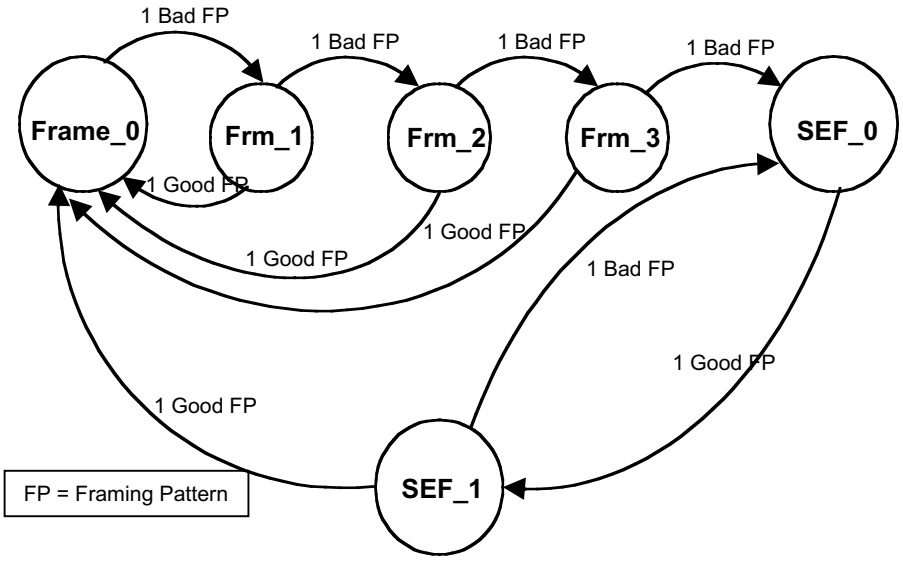
A Loss of Signal (LOS) state machine is used to indicate the absence of data signal on each channel. The in-sync state is regained upon correct reception of a number of consecutive frame alignment patterns. It is suggested that the LOS state machine follows the guidelines of ITU-T G.783 [9], section 6.2.1.1 . An example state machine where two correct frame alignment patterns are required to reach the in-sync state is shown in Figure 7.3.

Figure 7.3: Example TXLOS State Machine



A TXLOF state machine is used to declare an out-of-frame state based on the persistence of a Severely Errored Frame (SEF) condition for a specified length of time. The in-frame state is regained when the SEF condition has been terminated for a specified length of time. The use of SEF state machines and LOF criteria in accordance with ITU-T G.783 [9], section 6.2.5.1 is suggested. An example of such a SEF state machine is shown in Figure 7.4.

Figure 7.4: Example SEF State Machine



Although the SFI-5 IA states that the SFI-5 interface is data agnostic, elements of the SONET frame structure are required for the Converter to function properly.

7.1.2.3 BIP-8 Calculation

The section Bit Interleaved Parity (BIP-8) is calculated over the current SONET/SDH frame and compared against the B1 byte in the next received frame. BIP errors calculated in this way are accumulated in a counter in the IRB. Both scrambled and non-scrambled incoming B1 bytes are supported.

7.1.2.4 BIP-8 Generation

A BIP-8 byte is calculated for each of the 12 transmitter output channels and overwrites the next frame's corresponding A1 byte of column 60 for that channel. These bytes are labeled BC_n in the fiber transmission format shown in Table 7.1. The calculated BIP-8 for channel 0 overwrites $A1_{709}$ of the next frame, for channel 1 overwrites $A1_{710}$, etc.

Table 7.1: Transmission of STS-768 overhead framing bytes on 12 fibers

	1		59	60		64	65		69	70	
Fiber 0	X_1	- - - -	X_{697}	BC_0	- - - -	$A1_{757}$	$A2_1$	- - - -	$A2_{49}$	$A2_{61}$	- - - -
Fiber 1	X_2	- - - -	X_{698}	BC_1	- - - -	$A1_{758}$	$A2_2$	- - - -	$A2_{50}$	$A2_{62}$	- - - -
Fiber 2	X_3	- - - -	X_{699}	BC_2	- - - -	$A1_{759}$	$A2_3$	- - - -	$A2_{51}$	$A2_{63}$	- - - -
Fiber 3	X_4	- - - -	X_{700}	BC_3	- - - -	$A1_{760}$	$A2_4$	- - - -	$A2_{52}$	$A2_{64}$	- - - -
Fiber 4	X_5	- - - -	X_{701}	BC_4	- - - -	$A1_{761}$	$A2_5$	- - - -	$A2_{53}$	X_{65}	- - - -
Fiber 5	X_6	- - - -	X_{702}	BC_5	- - - -	$A1_{762}$	$A2_6$	- - - -	$A2_{54}$	X_{66}	- - - -
Fiber 6	X_7	- - - -	X_{703}	BC_6	- - - -	$A1_{763}$	$A2_7$	- - - -	$A2_{55}$	X_{67}	- - - -
Fiber 7	X_8	- - - -	X_{704}	BC_7	- - - -	$A1_{764}$	$A2_8$	- - - -	$A2_{56}$	X_{68}	- - - -
Fiber 8	X_9	- - - -	$A1_{705}$	BC_8	- - - -	$A1_{765}$	$A2_9$	- - - -	$A2_{57}$	X_{69}	- - - -
Fiber 9	X_{10}	- - - -	$A1_{706}$	BC_9	- - - -	$A1_{766}$	$A2_{10}$	- - - -	$A2_{58}$	X_{70}	- - - -
Fiber 10	X_{11}	- - - -	$A1_{707}$	BC_{10}	- - - -	$A1_{767}$	$A2_{11}$	- - - -	$A2_{59}$	X_{71}	- - - -
Fiber 11	X_{12}	- - - -	$A1_{708}$	BC_{11}	- - - -	$A1_{768}$	$A2_{12}$	- - - -	$A2_{60}$	X_{72}	- - - -

7.1.2.5 Byte Striping

With OC-768 framing information known, data is then byte striped across the 12 output channels one byte per channel with byte #1 of the OC-768 frame placed on channel 0, byte #2 placed on channel 1, etc. This is shown in Table 7.1, where X_n are the bytes reserved for future use [section 9.2.2.1 in reference 11].

7.1.2.6 PRBS Generator

The transmitter contains a PRBS generator capable of generating various PRBS patterns as required for system and chip level testing. The use and function of the PRBS generator are controlled through the IRB. The pattern is generated and striped across the 12 channels using the following procedure.

a. Seed an inverted PRBS23 (x^23+x^18+1=0) with (11100110000101111111111).
b. Column 71-51840, 1-58: The inverted PRBS fills column 71 to column 51840 in Fig. 7.5. Continue to fill column 1 through 58 of the next frame. All channels have identical PRBS bits. Bit #1 of PRBS23 is the first bit generated after the seed.
c. In column 59: Fill channels 0-7 with inverted A1's. Fill channels 8-11 with A1's.
d. Column 60: Fill with all zeroes in the first and second frames. In subsequent frames, fill with BC bytes calculated from the preceding frame.
e. Column 61-64: Fill with A1's.
f. Column 65-69: Fill with A2's.
g. Column 70: Fill channels 0-3 with A2's. Fill channels 4-11 with inverted A2's.

h. Reset the seed and repeat steps a-g.

The converter is also capable of generating special test patterns for optical jitter, extinction ratio and rise/fall time measurements. The detail is in Section 7.2.4.

Figure 7.5: PRBS Frame Format

	1		59	60		64	65		69	70	71	72		51840
Fiber 0	P_{51771}	---	$\overline{A1}_{697}$	BC_0	---	$A1_{757}$	$A2_1$	---	$A2_{49}$	$A2_{61}$	P_1	P_2	---	P_{51770}
Fiber 1	P_{51771}	---	$\overline{A1}_{698}$	BC_1	---	$A1_{758}$	$A2_2$	---	$A2_{50}$	$A2_{62}$	P_1	P_2	---	P_{51770}
Fiber 2	P_{51771}	---	$\overline{A1}_{699}$	BC_2	---	$A1_{759}$	$A2_3$	---	$A2_{51}$	$A2_{63}$	P_1	P_2	---	P_{51770}
Fiber 3	P_{51771}	---	$\overline{A1}_{700}$	BC_3	---	$A1_{760}$	$A2_4$	---	$A2_{52}$	$A2_{64}$	P_1	P_2	---	P_{51770}
Fiber 4	P_{51771}	---	$\overline{A1}_{701}$	BC_4	---	$A1_{761}$	$A2_5$	---	$A2_{53}$	$\overline{A2}_{65}$	P_1	P_2	---	P_{51770}
Fiber 5	P_{51771}	---	$\overline{A1}_{702}$	BC_5	---	$A1_{762}$	$A2_6$	---	$A2_{54}$	$\overline{A2}_{66}$	P_1	P_2	---	P_{51770}
Fiber 6	P_{51771}	---	$\overline{A1}_{703}$	BC_6	---	$A1_{763}$	$A2_7$	---	$A2_{55}$	$\overline{A2}_{67}$	P_1	P_2	---	P_{51770}
Fiber 7	P_{51771}	---	$\overline{A1}_{704}$	BC_7	---	$A1_{764}$	$A2_8$	---	$A2_{56}$	$\overline{A2}_{68}$	P_1	P_2	---	P_{51770}
Fiber 8	P_{51771}	---	$A1_{705}$	BC_8	---	$A1_{765}$	$A2_9$	---	$A2_{57}$	$\overline{A2}_{69}$	P_1	P_2	---	P_{51770}
Fiber 9	P_{51771}	---	$A1_{706}$	BC_9	---	$A1_{766}$	$A2_{10}$	---	$A2_{58}$	$\overline{A2}_{70}$	P_1	P_2	---	P_{51770}
Fiber 10	P_{51771}	---	$A1_{707}$	BC_{10}	---	$A1_{767}$	$A2_{11}$	---	$A2_{59}$	$\overline{A2}_{71}$	P_1	P_2	---	P_{51770}
Fiber 11	P_{51771}	---	$A1_{708}$	BC_{11}	---	$A1_{768}$	$A2_{12}$	---	$A2_{60}$	$\overline{A2}_{72}$	P_1	P_3	---	P_{51770}

7.1.2.7 High Speed Data Transmission

The data is output from the Converter toward the optical transmitter at a data rate of 3.318 Gb/s. Up to 1 ns of skew is allowed between the earliest and latest channels. Bytes are transmitted MSB first. The data transmitted is SONET scrambled data byte striped across 12 channels as described above. The Converter performs no additional encoding.

The signal levels for the 12 channel outputs are to be CML compatible for easy integration with optical module inputs and are intended to be AC coupled.

7.1.2.8 Optional TXCLK Output

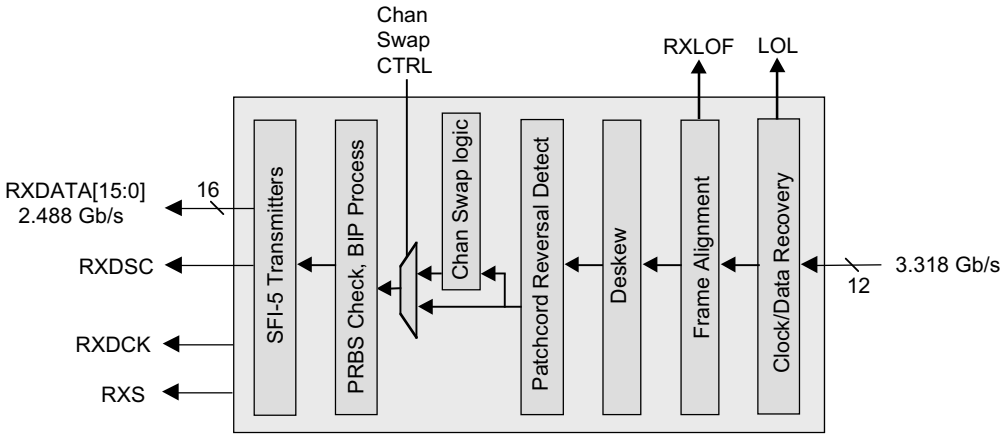
An optional clock output (TXCLK) with a nominal frequency of 829.5 MHz may be provided. TXCLK can be used to trigger the scope or BERT as indicated in 7.2.4.4.

7.1.3 Receiver Block

The receiver section of the Converter processes data in the receive direction, from optics to system. It receives 12 bit streams at 3.318 Gb/s each from the optical receiver, deskews and frames on the data in each channel, demultiplexes them into 16 bit streams, generates the RXDSC deskew reference channel and

RXS status channel and outputs the data in SFI-5 format. These basic functions are illustrated in Figure 7.6.

Figure 7.6: Basic receiver functional blocks



7.1.3.1 Clock/Data Recovery

Data at 3.318 Gb/s enters the Converter in the receive direction in the same 12 channel byte striped format as transmitted by the Converter in the transmit direction. Clock and data recovery is performed on each channel independently, and the clock recovered from channel 5 (channels are numbered from 0 to 11) is used as the basis for subsequent internal clocking requirements and as the basis for RXDCK.

The Converter IC includes functionality to ensure that a continuous Receive data clock (RXDCK) is sent to the framer device. The optical receiver lock range for each of the 12 channels will exceed 100ppm over temperature and supply range. The clock recovered from the received optical signal is compared with a clock derived from a reference frequency. Somewhere between 100ppm and 1000ppm, an out-of lock condition will be declared, and RXDCK shall switch from being sourced from the recovered clock to being sourced from the reference.

If loss of received data (LOS) is detected, then the RXDCK is sourced from the reference clock (RXREFCK).

Under conditions above when the RXDCK is not sourced from the received data, then the receive status alarm (RXS) will be set high.

Switching the receive data clock (RXDCK) shall be done such that the minimum pulse width and minimum period of RXDCK are not violated.

7.1.3.2 Frame Alignment

Frame alignment is obtained on all 12 channels through the detection of A1/A2 byte boundaries, which appear, on each channel.

A RXLOF state machine is used to declare an out-of-frame state based on the persistence of a Severely Errored Frame (SEF) condition for a specified length of time. The in-frame state is regained when the SEF condition has been terminated for a specified length of time. The use of SEF state machines and LOF criteria in accordance with ITU-T G.783 [9], section 6.2.5.1 , is suggested. An example of such a SEF state machine is shown in Figure 7.4 in the Frame and Byte Align section.

7.1.3.3 Deskewing

Data in the receive direction may have acquired up to a maximum of 40 ns of inter-channel skew, and the Converter must be capable of realigning such channels. The A1/A2 byte boundaries that appear on all channels form a convenient marker in each bit stream for use by FIFO's in the deskewing operation.

7.1.3.4 Patchcord Reversal Detection/Correction

The first 704 bytes of the STS-768 frame are reserved for future use. The next 4 are unscrambled A1 bytes, followed by 12 BIP-8 bytes, then 48 more unscrambled A1's, then 64 unscrambled A2 bytes. The next 704 bytes are reserved for future use. The transmitter maps these bytes onto the 12 fibers as shown in Table 7.1. Bytes labeled X in the figure are reserved for future use. The first byte of the OC-768 frame is always transmitted on and should be received on, Channel 0, as indicated in Table 7.1. Channels 8 – 11 contain five A1's, the rest contain only four. Similarly, channels 0 – 3 contain six A2's while the rest contain only five. If the receiver detects five A1's on channels 0 – 3 and six A2's on channels 8 – 11, patchcord reversal is detected. The converter chip has the ability to correct for this by swapping channel 0 for channel 11, channel 1 for channel 10, etc. The ability to perform automatic patchcord reversal correction may optionally be disabled through the IRB.

7.1.3.5 RXS Status Output

An asynchronous Receive Status signal is output on RXS. A binary 1 on RXS indicates that RXDATA and RXDCK are not derived from the receiver incoming data stream.

7.1.3.6 PRBS Checker

A PRBS checker that can be used to synchronize to and detect bit errors and synchronization errors in each channel's PRBS data stream initiated in section 7.1.2.6 is included. Errors are accumulated in IRB counters.

7.1.3.7 BIP-8 Calculation

The section Bit Interleaved Parity (BIP-8) is calculated over the current SONET/SDH frame and compared against the B1 byte in the next received frame. BIP errors calculated in this way are accumulated in a counter in the IRB. Both scrambled and non-scrambled incoming B1 bytes are supported. Also calculated is the BIP-8 for each of the twelve data channels. This is then compared to the BIP-8 data located in column 60 and errors are counted in the IRB.

7.1.3.8 RXDCK Output

The clock recovered from fiber data channel 5 (when numbered 0 through 11) is used to generate clocks for the remainder of the received data path in the Converter and is also the basis for the RXDCK output. The RXDCK output is nominally 622.08 MHz and is a requirement for an SFI-5 compliant interface. In the event of LOS on data channel 5, RXDCK is sourced from the RXREFCK input. If RXDCK as derived from the recovered channel clock deviates by more than 1000 ppm from RXREFCK, RXDCK will be sourced by RXREFCK. The source for RXDCK is switched from the recovered clock from fiber data channel 5 to RXREFCK as indicated in section 7.1.3.1.

7.1.3.9 RXDSC Channel Generation

The receiver generates the reference channel, which is subsequently output as RXDSC on the SFI-5 interface. The reference channel consists of Framing bytes, Expansion Header bytes and replicated data bytes from each of the 16 data channels, forming a frame of 1088 bits. The structure of the Reference Frame is shown in Table 7.2 for reference. Reference frames are continuously generated and output on RXDSC.

Table 7.2: Reference Channel RXDSC and TXDSC frame format

Bit time	Value	Value	Value	Value	Comments
1 - 32	A1 1111 0110	A1 1111 0110	A2 0010 1000	A2 0010 1000	Framing Bytes
33 - 64	EH1 1010 1010	EH2 1010 1010	EH3 1010 1010	EH4 1010 1010	Expansion Header bytes for future use.
65 - 96	R/TXDATA[15] bits 1 - 8	R/TXDATA[15] bits 9 - 16	R/TXDATA[15] bits 17 - 24	R/TXDATA[15] bits 25 - 32	64 consecutive bits from RXDATA[15] or TXDATA[15]
97 - 128	R/TXDATA[15] bits 33 - 40	R/TXDATA[15] bits 41 - 48	R/TXDATA[15] bits 49 - 56	R/TXDATA[15] bits 57 - 64	
129 - 160	R/TXDATA[14] bits 1 - 8	R/TXDATA[14] bits 9 - 16	R/TXDATA[14] bits 17 - 24	R/TXDATA[14] bits 25 - 32	64 consecutive bits from RXDATA[14] or TXDATA[14]
161 - 192	R/TXDATA[14] bits 33 - 40	R/TXDATA[14] bits 41 - 48	R/TXDATA[14] bits 49 - 56	R/TXDATA[14] bits 57 - 64	
193 - 1024					64 consecutive bits from R/TXDATA[14] to R/TXDATA[1]
1025 - 1056	R/TXDATA[0] bits 1 - 8	R/TXDATA[0] bits 9 - 16	R/TXDATA[0] bits 17 - 24	R/TXDATA[0] bits 25 - 32	64 consecutive bits from RXDATA[0] or TXDATA[0]
1057 - 1088	R/TXDATA[0] bits 33 - 40	R/TXDATA[0] bits 41 - 48	R/TXDATA[0] bits 49 - 56	R/TXDATA[0] bits 57 - 64	

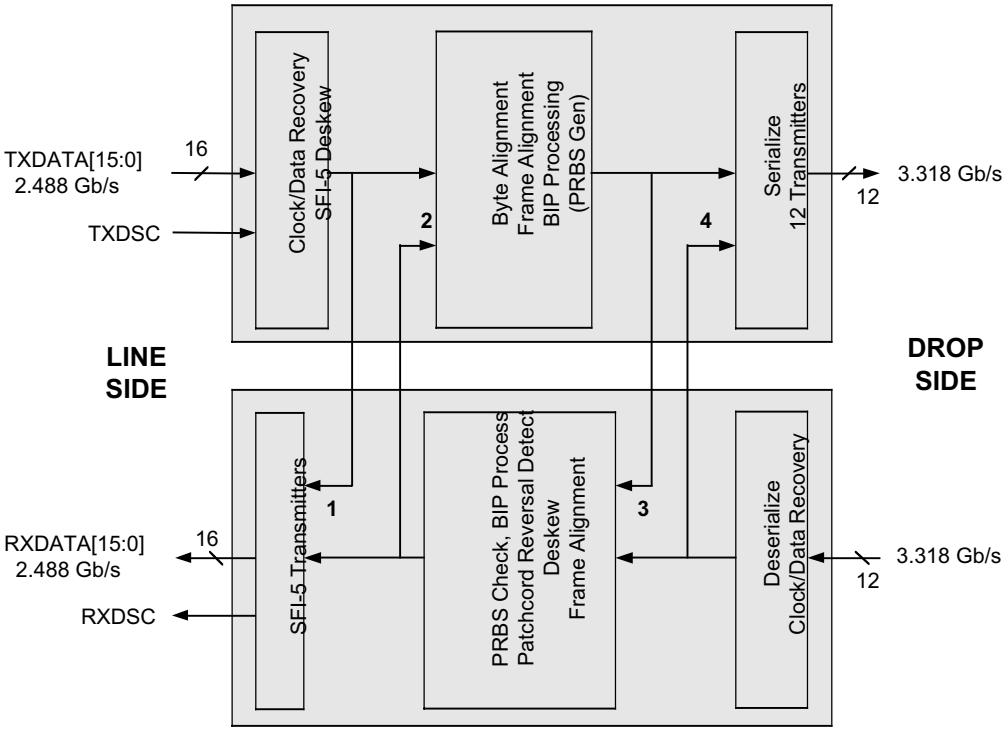
7.1.4 Internal Register Block (IRB)

The IRB is included for the purpose of error monitoring, pattern generation and to implement chip and system level test requirements. It is accessible by means of a standard two-wire interface.

7.1.5 Loopback Modes

The VSR converter supports four loopback modes as shown in Figure 7.7.

Figure 7.7: Loopback paths



7.1.5.1 Tx Line Side Loopback (1)

After SFI-5 deskew, the 16 channels of data are looped back to the receiver's SFI-5 outputs.

7.1.5.2 Tx Drop Side Loopback (3)

Before serialization, the Tx data is looped back to the receiver's frame alignment block.

7.1.5.3 Rx Line Side Loopback (2)

Before serialization and transmission on the receiver's SFI-5 outputs, the data is looped back to the transmitter's byte alignment block.

7.1.5.4 Rx Drop Side Loopback (4)

After deserialization, the received data is looped back to the transmitter's serializers.

7.1.6 AC and DC Electrical Characteristics

7.1.6.1 SFI-5 Electrical Characteristics

The Converter uses the same electrical levels and timing on the 2.488 Gb/s/channel interface as specified in the SxI-5 Implementation Agreement [1].

7.1.6.2 Converter Jitter Budget

The system jitter budget is based on the reference points in Figure 7.8. For a complete link analysis, this diagram is used with Table 7.3 and Table 7.7.

Figure 7.8: Block Diagram for Jitter Budget

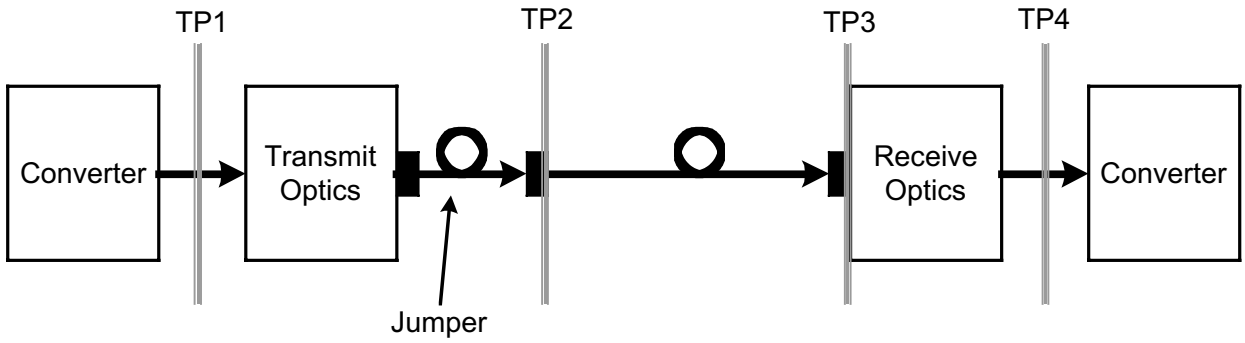


Table 7.3: Converter Jitter Budget

Compliance Point	Total Jitter		Deterministic Jitter		Skew	
	UI	ps	UI	Ps	UI	ns
TP1	0.24	72	0.08	24	3.3	1
TP4	0.70	211	0.32	96	133	40

7.1.7 Test Requirements

The Converter contains all the necessary functionality to comply with the test requirements for the SFI-5 interface as detailed in the SxI-5 Implementation Agreement [1].

7.2 Optical Interface Specifications

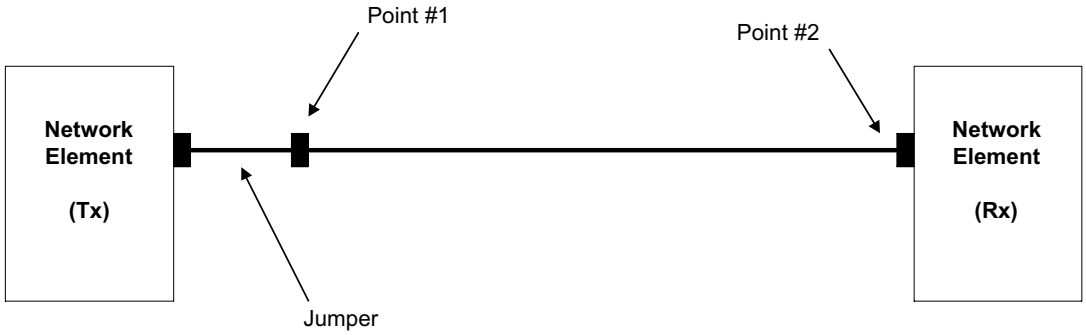
This section describes the optical physical layer for a full duplex electro-optic interface at the Physical Layer.

7.2.1 Optical interface requirements

Editor Notes: The optical link specifications rely heavily on the Gigabit Ethernet (GBE)methods [3] and 10 Gigabit Ethernet optical link model (Sections 10.1 and 10.2). The specifications listed in Section 7.2.1 are not identical to the 10GBE standard; i.e. the specifications have been modified to meet design constraints imposed by engineering 850nm parallel components. The extinction ratio specification has been adjusted for the reduced current swing requirements of laser arrays; crosstalk test conditions are added to reflect link performance for operation in a parallel environment; the data rate (3.318 Gb/s) differs from 10 Gigabit Ethernet. The values specified in this section are worst case, from start-of-life to end-of-life values and must be satisfied over the full range of operating conditions. Measured performance of BER<10^{12} shall be met for the worst case combination of values in the following specifications.

The OC-768 reference applications supported by this VSR interface are illustrated in Figure 6.1 and Figure 6.2. Measurements of the transmitter (Tx) and receiver (Rx) optical parameters are made at Point #1 and Point #2 respectively of the reference-cabling model illustrated in Figure 7.9. Point #1 occurs on a jumper 2 meters from the Tx.

Figure 7.9: Reference-cabling model for optical measurements



7.2.1.1 Transmitter specification

The transmitter for the VSR link shall have 12 lasers emitting into 12 separate fibers in a fiber ribbon cable. Each laser shall individually meet all the specifications listed in Table 7.4.

Table 7.4: Optical Transmitter Characteristics[1,2]

Parameter	Min	Max	Units
Signal Rate[3]	3.31776 +/- 20ppm		GBd
Pout	-8	-2	dBm
Extinction Ratio	6		dB
λc	830	860	nm
$\Delta\lambda$rms (Spectral Width)		0.65	nm
RIN[4]		-124	dB/Hz
t_r, t_f (20-80)		120	ps
Transmitter Skew[5]		5	ns

7.2.1.2 Receiver specification

The receivers for the VSR link shall have 12 receiving elements, one for each of the 12 separate fibers in the fiber ribbon cable. Each receiving element shall individually meet all the specifications listed in Table 7.5.

The receiver shall have a minimum roll-off of 20 dB per decade to filter out the transmitter high frequency noise.

[1] All transmitter specifications are per channel with all channels operating and at the end of a 2m patchcord.
[2] In the event of accidental transmitter-to-transmitter connection, no damage shall occur that will prevent the continued operation of the transmitter module within specification.
[3] All channels in a link run the same signal rate. Different links can have different rates within this specified range.
[4] Since it cannot be measured at the module level, RIN is an informative parameter to be guaranteed by the laser suppliers.
[5] Transmitter skew is the skew across the 12 channels when the converter input meets the SFI-5 Implementation Agreement.

Table 7.5: Optical Receiver Characteristics[6]

Parameter	Min	Max	Units
Signal Rate[3]	3.31776 +/- 20ppm		GBd
Electrical 3dB Upper Cutoff Frequency[7]	2500	4300	MHz
Rx Sensitivity[8]		-15	dBm
Rx Saturation[9]	-2		dBm
λc	830	860	nm
Total Link Reflection		-12	dB
Input Skew		35	ns
Signal detect asserted[10]		-17	dBm
Signal detect de-asserted	-31		dBm
Signal detect hysteresis	0.5		dB

7.2.1.3 Link power budget and penalties

The optical transmit and receive characteristics listed in Table 7.4 and Table 7.5 will support reference application 1 for 100 meters on 50/125μm MMF with fiber modal bandwidth of either 400MHz-km or 500MHz-km with acceptable margin. The informative link power budget presented in is based on the IEEE Ethernet spreadsheet, version 10GEPBud3_1_16.xls (see Appendices10.1 and 10.2) and shows the relevant parameters both for Reference Applications 1 and 2.

[6] All receiver specifications are per channel with all channels operating.

[7] The receiver shall have a minimum roll-off of 20 dB per decade to filter out the transmitter high frequency noise.

[8] The receiver sensitivity shall be such that the BER is $\leq 10^{-12}$ with the minimum optical power, worst case extinction ratio, and the maximum crosstalk possibility. The maximum crosstalk possibility is defined as the 'victim' receiver operating at its sensitivity limit and the remaining eleven 'aggressor' receivers operating at 6dB higher incident power.

[9] Since the saturation power decreases with increasing extinction ratio (ER), it should be measured at a maximum ER, a reasonable value being 12 dB

[10] Signal detect signal is asserted when all channels are active. Signal is de-asserted when one or more channel's power drops below threshold.

Table 7.6: Link Power Budget

Description	Value		Units
	Reference Application 1	Reference Application 2	
Fiber Type	Standard 50/125μm MMF	850nm laser optimized 50/125μm MMF	
Fiber modal BW	400/500[11]	2000	MHz-km
Operating distance	160	320	meters
Connector loss budget	0	2.0	dB
Link power budget	7.0	7.0	dB
Channel insertion loss	0.6	3.2	dB
Link power penalties	5.4	2.9	dB
Unallocated margin	1.0	0.9	dB

7.2.1.4 Jitter Specification

The compliance points for the jitter specification are illustrated in Figure 7.9. Note that point 1 and point 2 in the VSR reference cabling model of Figure 7.9 are equivalent to TP2 and TP3 respectively in the GBE specification (as well as Figure 7.8).

This VSR implementation shall conform to the jitter specification in Table 7.7.

Table 7.7: Optical Jitter Budget[12,13]

Compliance Point	Total Jitter		Deterministic Jitter[14]		Skew	
	UI	ps	UI	Ps	UI	ns
Point #1	0.45	136	0.21	63	16.6	5
Point #2	0.51	154	0.21	63	116	35

The receiver should be able to withstand wander as per Figure 7.10. (SJ refers to Sinusoidal Jitter), in the presence of high frequency jitter, where the total high frequency jitter does not exceed the total jitter defined for TP3.

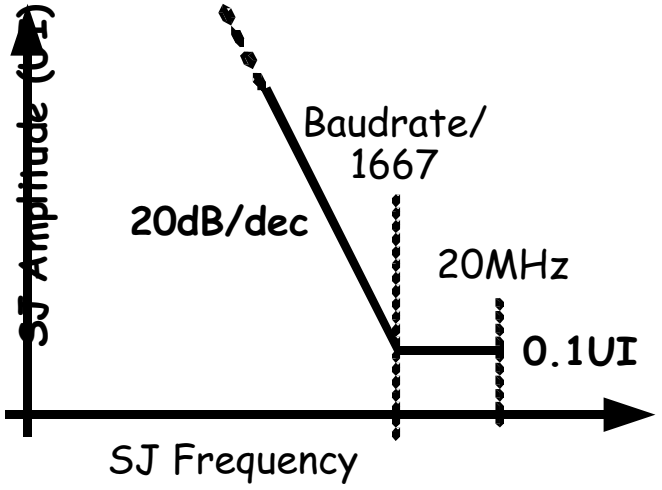
[11] In the link budget, the modal bandwidth for the overfilled launch 400/500 Mhz.km 50/125 μm fiber has been derated to an effective modal bandwidth of 350 Mhz.km. This is intended to account for modifications in the laser source and launch conditions, which differ from those for which the fiber was originally designed, specified, and intended.

[12] Measured using a recovered clock that is filtered with a single pole high pass filter with a corner frequency of baudRate/1667.

[13] RJ is calculated as being the difference between total jitter and deterministic jitter. RJ is allowed to be increased given a smaller DJ.

[14] The Duty Cycle Distortion (DCD) part of Deterministic Jitter shall be less than 0.1 UI.

Figure 7.10: Sinusoidal Jitter allowable amplitude vs. frequency



7.2.2 Optical fiber specification

This link is designed to work up to 100 meters over standard multimode fiber (MMF) ribbon cable with a modal bandwidth of $\geq$ 400 MHz-km. This link will also operate up to 300 meters using high-bandwidth (2000 MHz-km) MMF ribbon cable as shown in Table 7.8. To meet the skew spec at TP3, the ribbon cable shall have a maximum differential skew between fibers of 100 ps/m.

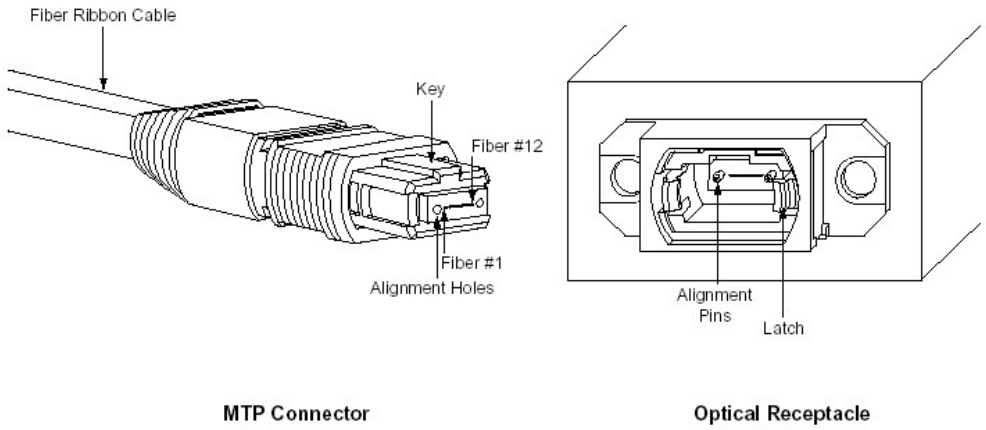
Table 7.8: Supported Fiber

Fiber type	Transmitter Launch Condition	Fiber Specification	Range (meters)
Standard 50/125μm	No launch condition specified	400 MHz-km @ 850nm[15]	2-160
Standard 50/125μm	No launch condition specified	500 MHz-km @ 850nm[15]	2-160
850-nm Laser optimized 50/125 μm	Encircled flux launch condition[16]	Per TIA/EIA-492AAAC	2-320

7.2.3 Connector Specification

The optical connector shall be the MTP® (MPO) with twelve multimode fiber terminations. The orientation of the terminated cable is "keyed" and conforms to IEC 61754-7 [4] as shown in Figure 7.11.

Figure 7.11: MTP® Connector



The maximum connector loss shall be 0.5 dB per mating. The OC-768 VSR receptacle contains male guide pins. MTP is a registered trademark of US Conec Ltd.

[15] Refer to IEEE 802.3-2002 section 38 to further describe this fiber.

[16] Specification is based on EIA/TIA-492AAAC Annex C: The encircled flux at 19um shall be greater than or equal to 86% and the encircled flux at 4.5um shall be less than or equal to 30% when measured into Type A1a (50/125μm multimode) fiber per TIA/EIA-455-203.

7.2.4 Measurement of the optical parameters

All transmitter measurements are to be made through a short patch cord of multimode fiber specified in Table 7.8, 2 meters in length. All referenced measurement techniques are scaled to 3.318Gb/s.

Depending on the parameters under test, the data pattern for measurement can be generated by the converter with an appropriate clock output for triggering or by an external signal generator such as a parallel BERT. The external signal pattern should be compatible with the 18-lanes (16 TXDATA, one TXDSC and one TXDCK) SFI-5 input data format or the 12-lane optical data format. In this case, it is recommended that the converter turn off the B1 and BC parity byte functions.

7.2.4.1 Center Wavelength and Spectral Width

The center wavelength and spectral width shall be measured per EIA/TIA-455-127 using a pure PRBS31 from the converter.

7.2.4.2 Optical power measurements

The optical power shall be measured as in [5, Sec. 38.6.2.] The measurement shall be made per EIA/TIA-455-95A using the pattern described in Section 7.2.4.1.

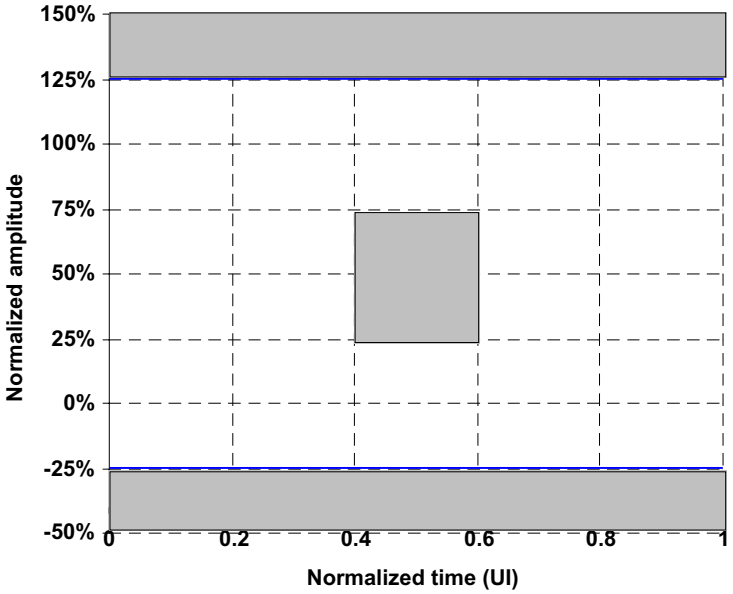
7.2.4.3 Extinction Ratio Measurements

The extinction ratio shall be measured as in [6]. This measurement may be made per EIA/TIA-526-4A using a square pattern consisting of four to eleven ones followed by an equal run of zeros. The converter shall generate this pattern.

7.2.4.4 Eye Mask Test

In order to ensure interoperability among vendor components and systems, an eye mask test shall be performed. The filtered eye shall meet the eye mask specification in Figure 7.11 and shall be measured as in [5, Sec. 38.6.5] using the pattern described in * MERGEFORMAT Section 7.2.4.1. The converter output clock, if present, can be used to trigger the scope or BERT. Alternatively, the trigger can be recovered from the data using a golden PLL.

Figure 7.12: 12 Channel Eye Mask



7.2.4.5 Transmitter Rise/Fall Characteristics

The transmit rise/fall characteristics shall be measured as [5, Sec. 38.6.6] using the square pattern described in Section 7.2.4.3.

7.2.4.6 Receiver Sensitivity Measurements

The receivers shall be tested for sensitivity as in [5, Sec. 38.6.7] by forcing the following conditions at Point #2 on Figure 7.9 and observing results at SFI-5. A parallel BERT with 3.318 Gbps signal drives an ideal low-noise, high-speed laser source with the worst case extinction ratio of 6 dB. The jitter test pattern described in Section 7.2.4.8 is generated by the BERT and the corresponding optical signal is injected into the receive channel under test. Using loopback #4 in Figure 7.7, the data are routed to the optical transmitter, then to a low-noise golden receiver. The BER is analyzed by the BERT to calculate the receiver sensitivity. Additionally the crosstalk requirement dictates that all the eleven aggressor channels be actively driven by similar data patterns at an average power level 6dB higher than the sensitivity limit. * MERGEFORMAT

Alternatively, a PRBS from the BERT compatible with that from the converter PRBS generator can be sent to the receiver. With the signal source providing a clock to the converter, the bit error rate can be measured with the converter internal PRBS checker. Since this does not test the full receiver, it is informative.

7.2.4.7 Receiver 3dB electrical upper cutoff frequency

The receiver 3dB electrical upper cutoff frequency shall be measured as in [5, Sec. 38.6.12] using the jitter test pattern and the loopback procedure described in Section 7.2.4.6.

7.2.4.8 Jitter measurements

The jitter measurements shall be measured using the BER Bathtub method as in [5, Sec. 38.6.8 and 38.6.9].

Since the SONET data format is different from that of the Ethernet, a test pattern with the following attributes is needed.

a. Ease of implementation.
b. Compatibility with BERT measurement systems.
c. Reasonable test time.
d. Provide a high transition density for eye pattern measurement.
e. Provide a low transition density to test converter CDR and optical jitter. 72 continuous identical digits (CID) is need for stringent SONET up-time requirements.
f. Provide a line balance to emulate operational environment.
g. Provide a realistic cross talk environment.

The following procedure provides such a pattern.

a. Generate PRBS15 seeded with 15 “1”s using $x^{15} + x^{14} + 1 = 0$ with an inverted output.[17]
b. Replace 144 bits from bit #852 to #995 of this PRBS with the following 145 bits[18].
   16x(01), 72x(0), (10111110), 16x(01), (0).
   Fill the channel of a frame, ie., bytes 1-51840, with this pattern.
c. Reset the seed with 15 “1”s and generate PRBS15 using $x^{15} + x^{14} + 1 = 0$ with an inverted output.
d. Replace 144 bits from bit #852 to #995 of this PRBS with the following 145 bits.
   16x(10), 72x(1), (01000001), 16x(10), (1).
   Fill the channel of a frame, ie., bytes 1-51840, with this pattern.
e. Repeat a-d above.

To provide cross talk and the possibility of simultaneously testing all channels, the above pattern or a pure PRBS15 shall be applied to all channels. However,

[17] Bit #1 of PRBS15 is the first bit generated after seeding with 15 "1"s

[18] This results in a block length of 2^{15} bits. This is required by a parallel BERT which only allows programmed block length with integral multiple of 2^n, where n may be vendor specific. The replacement site in PRBS15 is chosen because it does not have extreme transition densities.

to avoid unrealistically severe cross talk, the special patterns in adjacent channels shall be delayed by 80 bits. With the above data pattern generated by the converter, the BER bathtub can be measured using a parallel BERT programmed to accept the incoming pattern.

Table 7.9: 12 Channel Parallel Section Normative/Informative Matrix

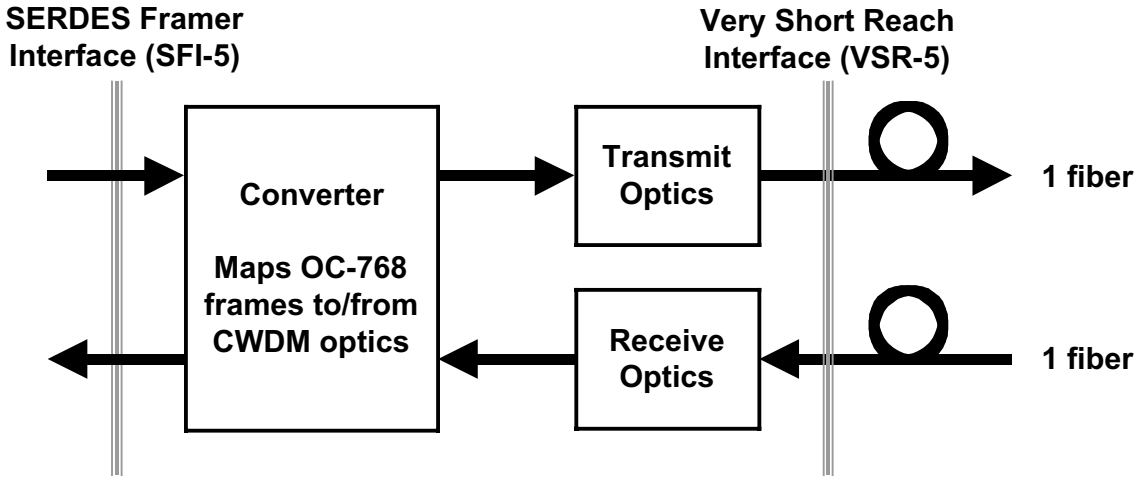
Paragraph	Topic	Normative/Informative
7.1.1	Converter	Normative
7.1.2	Transmitter Block	Informative
7.1.2.1	Data Recovery and SFI-5 deskew	Informative
7.1.2.2	Frame and Byte Align	Informative
7.1.2.3	BIP-8 Calculation	Informative
7.1.2.4	BIP-8 Generation	Normative
7.1.2.5	Byte Striping	Normative
7.1.2.6	PRBS Generator	Normative
7.1.2.7	High speed data transmission	Normative
7.1.2.7	Electrical Characteristics	Informative
7.1.2.8	Optional TXCLK Output	Informative
7.1.3	Receiver Block	Informative
7.1.3.1	Clock/Data Recovery	Informative
7.1.3.2	Frame Alignment	Informative
7.1.3.3	Deskewing	Normative
7.1.3.4	Patchcord Reversal	Informative
7.1.3.5	RXS Status Output	Normative
7.1.3.6	PRBS Checker	Normative
7.1.3.7	BIP-8 Calculation	Informative
7.1.3.8	RXDCK Output	Informative
7.1.3.9	RXDSC Channel Generation	Normative
7.1.4	Internal Register Block	Informative
7.1.5	Loopback Modes	Informative
7.1.6	AC and DC Electrical Characteristics	Informative
7.1.7	Test requirements	Normative
7.2.1	Optical Reference points	Normative
7.2.1.1	Transmitter Specifications	Normative
7.2.1.2	Receiver Specifications	Normative
7.2.1.3	Link Power Budget	Informative
7.2.1.4	Jitter Specifications	Normative
7.2.2	Optical Fiber Specification	Normative
7.2.3	Optical Connector Specification	Normative
7.2.4	Measurement of Optical Parameters	Normative

8 FOUR CHANNEL CWDM

This OC-768 VSR interface utilizes CWDM optics technology with a four channel array of 1300nm lasers based on a 64b/66b Gearbox. It addresses reference applications 1, 2, 3, and 4 operating at 10.264 Gb/s without FEC and 11.09 Gb/s for the G. 709 FEC rate. The target performance of the VSR interface is to provide a link for a SONET/SDH OC-768 scrambled data stream over standard duplex single mode fiber at distances up to 2 kilometers.

The OC-768 VSR interface is a bi-directional interface. A functional block diagram is illustrated in Figure 8.1.

Figure 8.1: Functional block diagram of four channel CWDM interface.



The transmit direction includes a Converter, laser driver, and four 1300nm lasers, which are coupled onto a single fiber using a CWDM multiplexer, supporting a distance up to 2 kilometers. The Converter receives signals from a 16 bit wide data bus at 2.488 up to 2.7725 Gb/s per channel from an external OC-768 Framer or G.709 FEC Processor utilizing the SFI-5 electrical interface. The 16 bit parallel bus is mapped onto 4 channels at 10.264 Gb/s up to 11.09 Gb/s. The four channels are forwarded to the CWDM multiplexer subassembly, which converts the four electrical signals to four optical wavelengths at 10.264 to 11.09 Gb/s and combines them onto a single fiber.

The CWDM optical interface receives the four optical signals from the single mode fiber at a data rate of 10.264 to 11.09 Gb/s per channel. The CWDM receiver subassembly converts the four optical signals to four electrical signals. These four electrical signals are deconstructed into a 16 bit wide data stream by

the Converter for connection to the external OC-768 framer chip using the SFI-5 electrical interface.

The SERDES -Framer Interface for OC-768 (SFI-5) shown in the block diagram in Figure 8.1 is compliant with the OIF SFI-5 specification but limited to SONET/SDH or G .709 framed data at the nominal data rate of 2.488 to 2.7725 Gb/s.

8.1 Converter

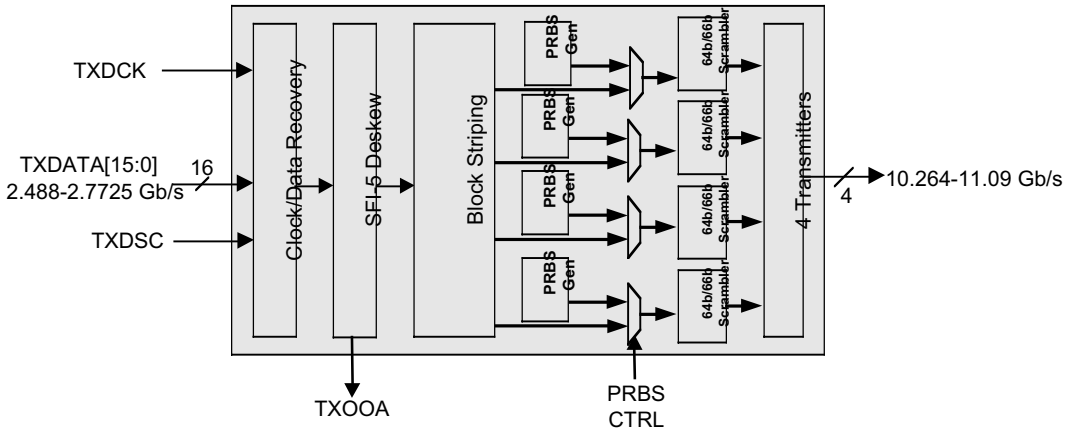
8.1.1 General Description

The Converter performs the general function of mapping an SFI-5 datastream to four channels for output to CWDM transmit optics in the transmit direction. It also performs the reverse function of receiving four channels of data from a CWDM optical receiver and mapping the data into an SFI-5 datastream in the receive direction. In order to perform these functions the Converter contains all the digital circuitry necessary for deskewing data in both directions, frame and byte alignment, state machine logic, as well as the analog circuitry required for clock and data recovery and clock generation for all internal and external requirements and for all signal inputs and outputs. Also included is an Internal Register Block (IRB), accessible through a two-wire interface, which is used to implement test requirements for the SFI-5 and optics interfaces as well as various performance monitoring and counting functions.

8.1.2 Transmitter Block

The transmitter section of the Converter processes data in the transmit direction, from system to optics. It receives data in SFI-5 format at 2.488 Gb/s to 2.7725 Gb/s per channel, deskews the data channels, block stripes the data, scrambles the data, then outputs the data on four channels to the transmit optics operating at 10.264 to 11.09 Gb/s. These functions are outlined in Figure 8.2.

Figure 8.2: Transmitter Functional Blocks



8.1.2.1 Data Recovery and SFI-5 Deskew

The transmitter recovers data independently on TXDATA[15:0] and TXDSC at 2.488 to 2.7725 Gb/s per channel as described in the SFI-5 Implementation Agreement [1].

Data recovered on TXDATA[15:0] have up to the maximum amount of relative skew between them as is allowed by the SxI-5 specification. Data on the latest channel may lag data on the earliest channel by up to the specified number of UI. Bit lane deskew is accomplished with the TXDSC channel. TXDSC is a reference channel containing replicated data from each of the 16 data channels in a frame format described in the SFI-5 IA. The SFI-5 Interface and Deskew blocks contain the buffers, deskew controllers and delay elements necessary for lane-to-lane data deskewing. By comparing the data on each channel with its corresponding data on TXDSC, the skew between data and reference channel is deduced. Once the delay is known the delay element associated with that channel is adjusted for alignment between the data and reference channel. This is carried out on each channel successively until all data channels are deskewed relative to the reference channel and therefore relative to each other.

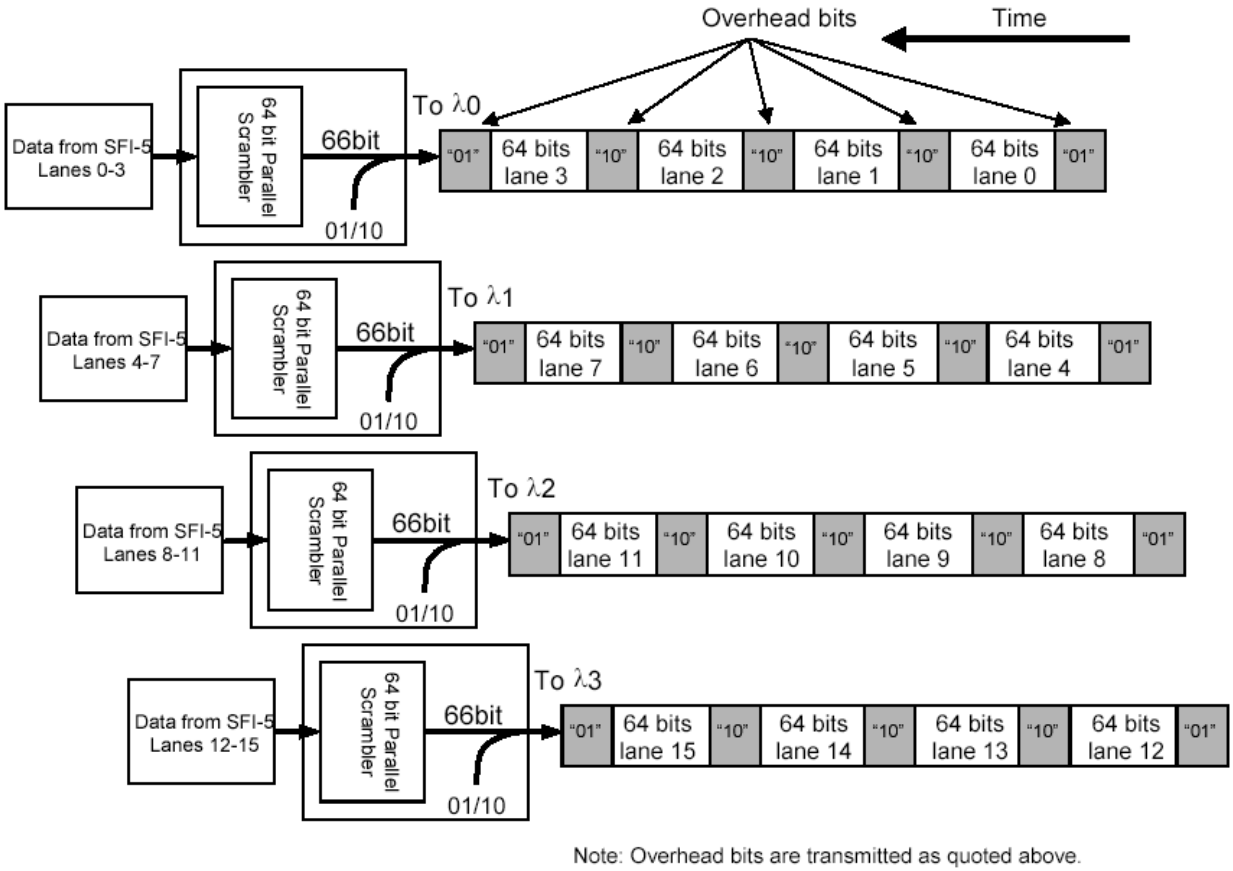
An out-of-alignment alarm TXOOA is set if pattern matching cannot be achieved on all 16 channels, and is cleared when it is achieved. After successfully deskewing the 16 channels, the skew on each channel is continuously monitored, allowing the Converter to track skew changes of up to the maximum amount allowed in the SFI-5 IA without introducing errors. A set of counters in the IRB is allocated for counting the instances of pattern mismatch between each channel's data and the corresponding data on the deskew channel. The SFI-5 IA contains greater detail on the deskewing algorithm and TXDSC frame format.

8.1.2.2 Frame and Byte Align

After de-skew, data from SFI-5 lanes 0 to 15 are block striped in groups of 64 bits from each lane. Each 64 bits of data is scrambled with $1+X^{39}+X^{58}$. Data from the first four lanes (0,1,2,3) of SFI-5 are striped into λ0, data from lanes (4, 5, 6, 7) into λ1, data from lanes (8, 9, 10, 11) into λ2, and data from lanes (12, 13, 14, 15) into λ3. The Converter uses 64b/66b code to transmit data over 4 lanes with frame boundaries defined by 01 and 10 overhead bits. Receive byte alignment is accomplished by locating a start of frame bits 01 marker followed by succession of three 10 bits, then followed by start frame 01 pattern.

The marker bits are separated by 64 bits of scrambled data on each wavelength. Four blocks consisting of 64 bits of data originating from the first four SFI-5 lanes (0,1,2,3) are mapped into wavelength 0, the next four lanes (4,5,6,7) are mapped into the wavelength 1 and so forth with the last 4 lanes from SFI-5 mapped into wavelength 3. The receiver follows the same mapping from wavelength channel to SFI-5. They are mapped according to the diagram in Figure 8.3.

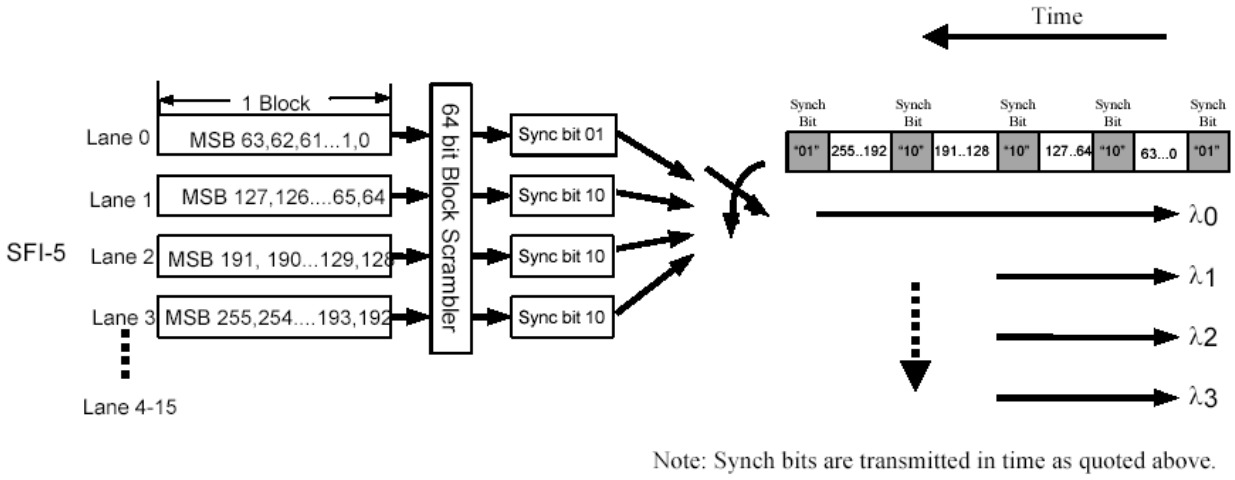
Figure 8.3: Transmission of OC-768 framing over four wavelengths.



8.1.2.3 VSR-5 Four-channel Data Striping with 64b/66b

As shown in Figure 8.4, SFI-5 are block striped with 64 bits from each lane of SFI-5. Data transmission starts with 01 sync bits, followed by 64 bits of data from each SFI-5 lane starting with bit 0 from lane 0 and ending with bit 63 from lane 3 striped in to wavelength 0. The second coder not shown in the diagram stripes data from lane 4-7 in to wavelength 1, and so on for wavelengths 2 and 3. After transmission of first frame, the next three frames are sent with sync pattern 10 to allow 120 bits of absolute skew between any channels.

Figure 8.4: Four-channel Data Striping with 64b/66b encoding on TX side



Note: Synch bits are transmitted in time as quoted above.

8.1.2.4 PRBS Generator

The transmitter contains a PRBS generator capable of generating various PRBS patterns as required for system and chip level testing. The use and function of the PRBS generator are controlled through the IRB. The PRBS pattern is injected into the entire 64b/66b frame. At a minimum a PRBS 2^{31}-1 pattern is supported. The generated PRBS bytes are replicated within the frame as shown in Table 8.1 with the PRBS bytes labeled P_n. The generating polynomial used for the PRBS 2^{31}-1 pattern is $x^{31} + x^{28} + 1 = 0$ with an inverted output.

The PRBS pattern is replicated on wavelengths 0 through 3 after each sync byte, for 8 consecutive bytes followed by a sync byte, subsequent PRBS bytes are replicated on wavelengths 0 through 3. This pattern is displayed in Table 8.1. A start seed of 31 consecutive zeros is specified for the first 31 bits of the 8 consecutive bytes transmitted after the first sync bit shown in Table 8.1.

Table 8.1: PRBS Frame Format

Sync	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	Byte7	Byte8	Sync	155520

λ_0	'01	P_1	P_2	P_3	P_4	P_5	P_6	P_7	P_8	'10	- - -	P_{155312}
λ_1	'01	P_1	P_2	P_3	P_4	P_5	P_6	P_7	P_8	'10	- - -	P_{155312}
λ_2	'01	P_1	P_2	P_3	P_4	P_5	P_6	P_7	P_8	'10	- - -	P_{155312}
λ_3	'01	P_1	P_2	P_3	P_4	P_5	P_6	P_7	P_8	'10	- - -	P_{155312}

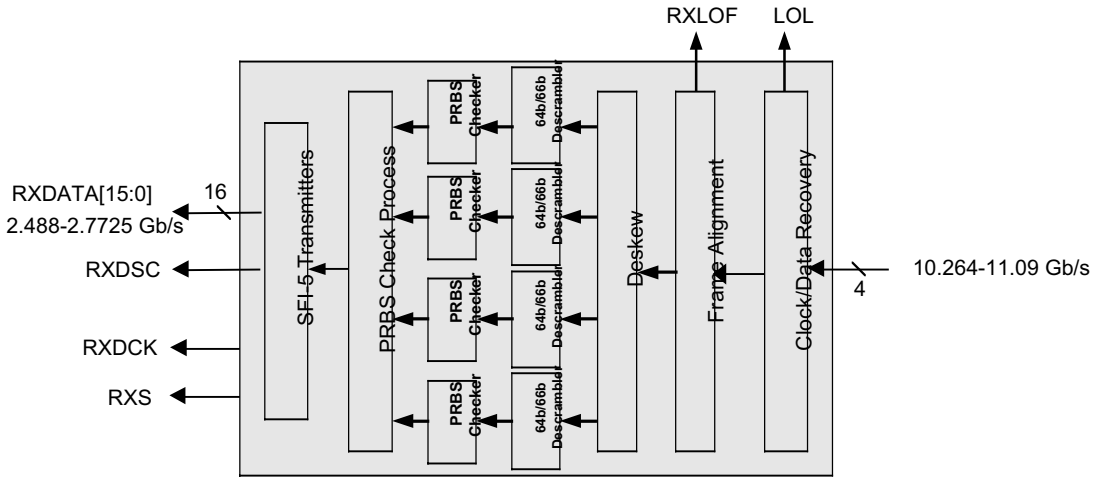
8.1.2.5 High Speed Data Transmission

The data output from the Converter to the optical transmitter operate at data rate of 10.264 to 11.09 Gb/s. Up to 120 bits of skew is allowed between the earliest and latest channels. The signal levels for the four channel outputs are to be CML compatible for easy integration with optical module inputs and are intended to be AC coupled.

8.1.3 Receiver Block

The receiver section of the Converter processes data in the receive direction, from optics to system. It receives four-bit streams at 10.264 to 11.09 Gb/s from each optical receiver, deskews and frames on the data in each channel, demultiplexes them into 16 bit streams, generates the RXDSC deskew reference channel and RXS status channel and outputs the data in SFI-5 format. These basic functions are illustrated in Figure 8.5.

Figure 8.5: Basic receiver functional blocks.



8.1.3.1 Clock/Data Recovery

Data at 10.264 to 11.09 Gb/s enters the Converter in the receive direction in the same 4-channel byte striped format as transmitted by the Converter in the transmit direction. Clock and data recovery is performed on each channel independently, and the common clock recovered from channel 1 (channels are

numbered from 0 to 3) is used as the basis for subsequent internal clocking requirements and as the basis for RXDCK.

The Converter IC includes functionality to ensure that a continuous Receive data clock (RXDCK) is sent to the FEC processor or framer device. The optical receiver lock range for each of the channels will exceed 100ppm over temperature and supply range. The clock recovered from the received optical signal is compared with a clock derived from a reference frequency. If the recovered clock deviates from the reference frequency by more that 1000ppm, then RXDCK will switch from being sourced from the recovered clock to the reference clock (RXREFCK). Somewhere between 100ppm and 1000ppm, an out-of lock condition will be declared, and RXDCK shall switch from being sourced from the recovered clock to being sourced from the reference.

If loss of received data (LOS) is detected, then the RXDCK is sourced from the reference clock (RXREFCK).

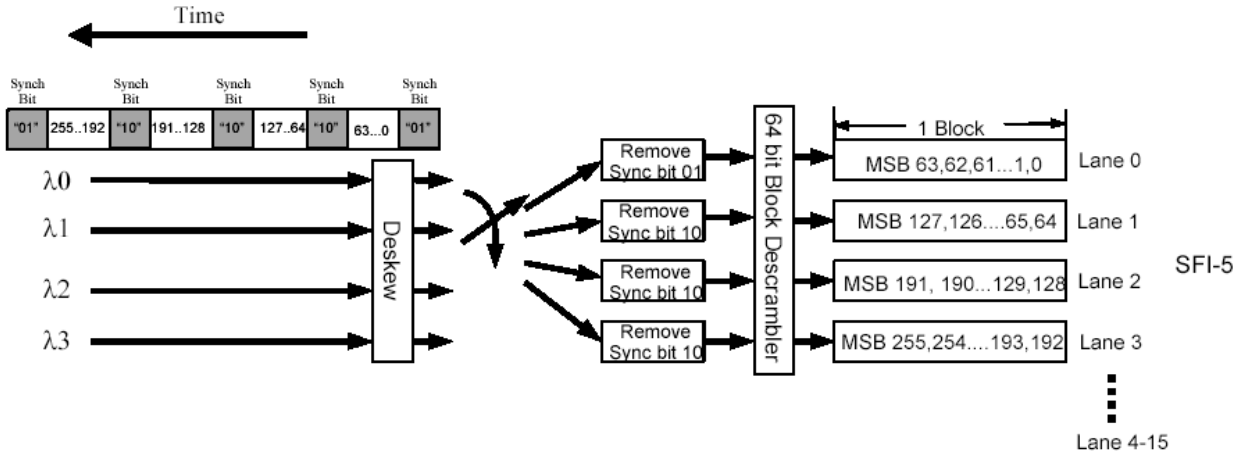
Under conditions above when the RXDCK is not sourced from the received data, then the receive status alarm (RXS) will be set high.

Switching the receive data clock (RXDCK) shall be done such that the minimum pulse width and minimum period of RXDCK are not violated.

8.1.3.2 Frame Alignment and Deskew

Frame alignment and deskew is obtained on all four channels through the detection of 64b/66b “01” and “10” bit boundaries, which appear, on each channel. Figure 8.6 details the operation of the receiver showing alignment and the 64b/66b decoder.

Figure 8.6: Frame Alignment and Deskew of data



An RXLOF condition is declared when an out-of-frame state based on the persistence of a Severely Errored Frame (SEF) is met. This condition is declared when 16 or more bad frame syncs out of 64 frames occurs. The in-frame state is regained when the SEF condition has been terminated for 64 consecutive error-free frames. An example of such a SEF state machine is shown in Figure 8.7in the Loss of Frame section.

Data in the receive direction may have acquired up to a maximum of 120 bits of inter-channel skew, and the Converter must be capable of realigning such channels. The 01 and 10 byte boundaries that appear on all channels form a convenient marker in each bit stream for use by FIFO's in the deskewing operation.

8.1.3.3 Scrambler

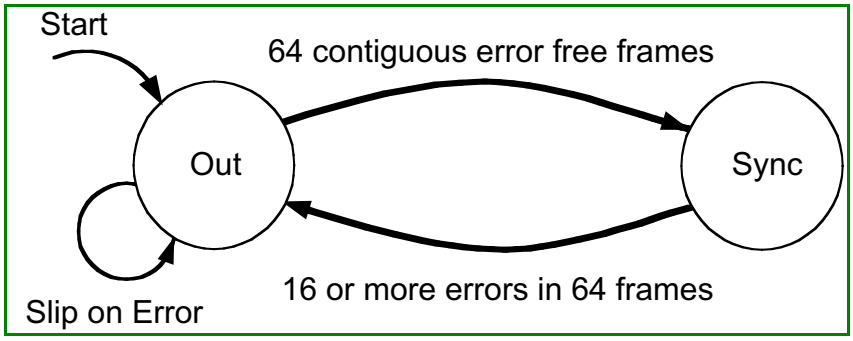
Block data 64bits long are fed in to the de-scrambler in the round robin. The scrambler is self synchronous based on $1+X^{39}+X^{58}$.

8.1.3.4 Loss of Synchronization

A Loss of Frame (LOF) state machine is used to indicate the absence of the data signal on a channel. With a frame defined as 64 bits plus the header bits, the LOF state is reached when 16 or more errored frames are received – this is the SEF, or severely errored frame condition. When 64 contiguous error free frames are received, the receiver is in sync.

The Severely Errored Frame (SEF) condition is based on the detection of the overhead sync bits in their proper location. The receiver looks for presence of “01” sync bits on a 66 bit boundary, followed by three frames with “10” bits. The demux looks for the “10” and “01” pattern repeating every 256 bits, the de-mux phase may be slipped by one bit until “10” and “01” frame bits are in sync. Frames are considered in error when the sync bit boundaries are not found to be their expected value. When 16 sync bits are found in error, the SEF condition is met. When 64 sync bits are found to be their expected value the SEF condition is removed and the receiver is in sync. Figure 8.7 shows an example state machine.

Figure 8.7: Example TXLOF State Machine



A TXLOF state machine is used to declare an out-of-frame state based on the persistence of 32 or more errors on 64 of a Severely Errored Frame (SEF).

8.1.3.5 RXS Status Output

An asynchronous Receive Status signal is output on RXS. A binary 1 on RXS indicates that the deskewing process is either in progress or has not been successful. A binary 0 indicates successful deskewing of the four channel interface.

8.1.3.6 PRBS Checker

A PRBS checker that can be used to synchronize to and detect bit errors and synchronization errors in each channel's PRBS data stream initiated in the transmitter section of a Converter is included. Errors are accumulated in IRB counters.

8.1.3.7 RXDCK Output

The clock recovered from wavelength channel 1 (when numbered 0 through 3) is used to generate clocks for the remainder of the received data path in the Converter and is also the basis for the RXDCK output. The RXDCK output is nominally 622.08 MHz. In the event of LOF on data channel 2, RXDCK is sourced from the RXREFCK input. If RXDCK as derived from the recovered channel clock deviates by more than 1000 ppm from RXREFCK, RXDCK will switch to being sourced by RXREFCK.

8.1.3.8 RXDSC Channel Generation

The receiver generates the reference channel, which is subsequently output as RXDSC on the SFI-5 interface. The reference channel consists of Framing bytes, Expansion Header bytes and replicated data bytes from each of the 16

data channels, forming a frame of 1088 bits. The structure of the Reference Frame is shown in Table 8.2 for reference. Reference frames are continuously generated and output on RXDSC.

Table 8.2: Reference Channel RXDSC and TXDSC frame format

Bit time	Value	Value	Value	Value	Comments
1 - 32	A1 1111 0110	A1 1111 0110	A2 0010 1000	A2 0010 1000	Framing Bytes
33 - 64	EH1 1010 1010	EH2 1010 1010	EH3 1010 1010	EH4 1010 1010	Expansion Header bytes for future use.
65 - 96	R/TXDATA[15] bits 1 - 8	R/TXDATA[15] bits 9 - 16	R/TXDATA[15] bits 17 - 24	R/TXDATA[15] bits 25 - 32	64 consecutive bits from RXDATA[15] or TXDATA[15]
97 - 128	R/TXDATA[15] bits 33 - 40	R/TXDATA[15] bits 41 - 48	R/TXDATA[15] bits 49 - 56	R/TXDATA[15] bits 57 - 64	
129 - 160	R/TXDATA[14] bits 1 - 8	R/TXDATA[14] bits 9 - 16	R/TXDATA[14] bits 17 - 24	R/TXDATA[14] bits 25 - 32	64 consecutive bits from RXDATA[14] or TXDATA[14]
161 - 192	R/TXDATA[14] bits 33 - 40	R/TXDATA[14] bits 41 - 48	R/TXDATA[14] bits 49 - 56	R/TXDATA[14] bits 57 - 64	
193 - 1024					64 consecutive bits from R/TXDATA[14] to R/TXDATA[1]
1025 - 1056	R/TXDATA[0] bits 1 - 8	R/TXDATA[0] bits 9 - 16	R/TXDATA[0] bits 17 - 24	R/TXDATA[0] bits 25 - 32	64 consecutive bits from RXDATA[0] or TXDATA[0]
1057 - 1088	R/TXDATA[0] bits 33 - 40	R/TXDATA[0] bits 41 - 48	R/TXDATA[0] bits 49 - 56	R/TXDATA[0] bits 57 - 64	

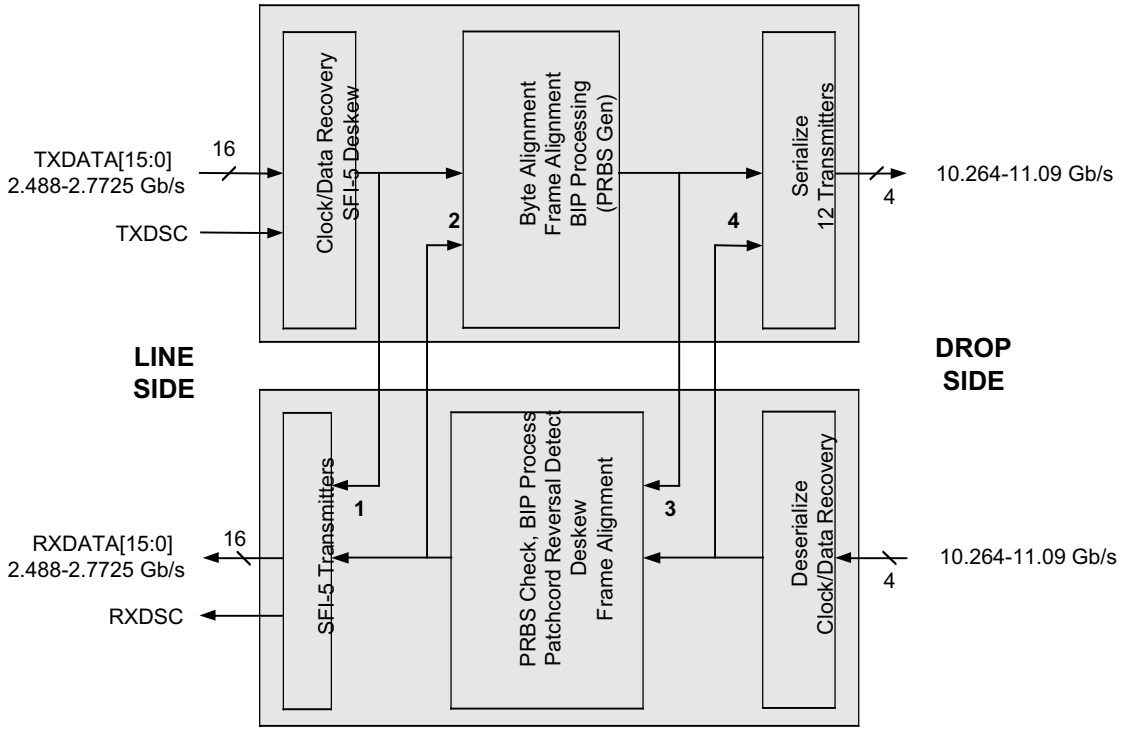
8.1.4 Internal Register Block (IRB)

The IRB is included for the purpose of error monitoring, pattern generation and to implement chip and system level test requirements. It is accessible by means of a standard two-wire interface.

8.1.5 Loopback Modes

The VSR converter supports four loopback modes as shown in Figure 8.8.

Figure 8.8: Loopback paths



8.1.5.1 Tx Line Side Loopback (1)

After SFI-5 deskew, the 16 channels of data are looped back to the receiver's SFI-5 outputs.

8.1.5.2 Tx Drop Side Loopback (3)

Before serialization, the Tx data is looped back to the receiver's frame alignment block.

8.1.5.3 Rx Line Side Loopback (2)

Before serialization and transmission on the receiver's SFI-5 outputs, the data is looped back to the transmitter's byte alignment block.

8.1.5.4 Rx Drop Side Loopback (4)

After deserialization, the received data is looped back to the transmitter's serializers.

8.1.6 SFI-5 Electrical Characteristics

The Converter uses the same electrical levels and timing on the 16 channel interface as specified in the SxI-5 Implementation Agreement.

8.1.7 Test Requirements

The Converter contains all the necessary functionality to comply with the test requirements for the SFI-5 interface as detailed in the SxI-5 Implementation Agreement.

8.2 Optical Interface Specifications

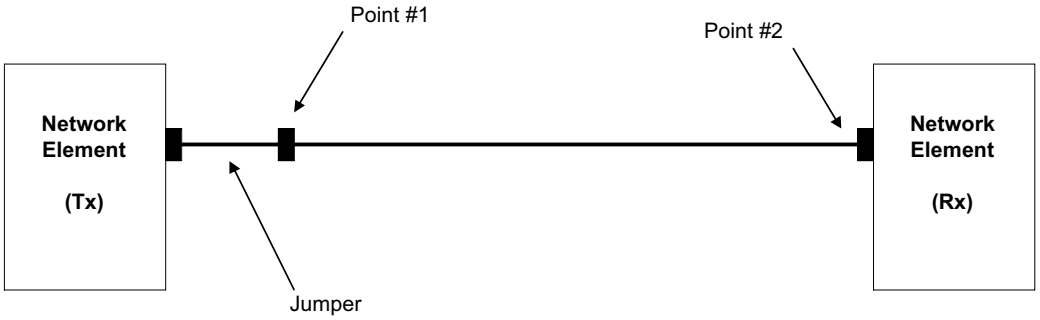
This section describes the optical physical layer for a full duplex electro-optic interface at the Physical Layer.

8.2.1 Optical Interface Requirements

Editor Notes: The optical link specifications rely heavily on the Gigabit Ethernet standard [3] and the corresponding Gigabit Ethernet optical link model included in Section 10.3. The specifications listed in Sec. 8.2 are not identical to the GBE standard; i.e. the specifications have been modified where necessary to meet design constraints imposed by engineering CWDM components. The extinction ratio specification has been adjusted for the reduced current swing requirements of lasers; a crosstalk immunity measurement was added to prevent link performance degradation due to operation in a CWDM environment. The Gigabit Ethernet link, included in Section 10.3, has been used to model all changes in the values from the original Gigabit Ethernet specifications [3]. The values specified in this section are worst case, end-of-life values and must be satisfied over the full range of operating conditions. The optical link design objective of a BER<10-12 shall be met for the worst case combination of values in the following specifications.

The OC-768 reference applications supported by this VSR interface are illustrated in Figure 6.1, Figure 6.2, and Figure 6.3. Figure 6.2 shows the maximum of four connectors allowed in the link. Measurements of the transmitter (Tx) and receiver (Rx) optical parameters are made at Point #1 and Point #2 of the reference-cabling model illustrated in Figure 7.9. Point #1 occurs on a jumper 2 meters from the Tx. Conditions for testing the receiver (Rx) optical parameters are made at Point #2. All measurements described in Section 8.2.3 are made at these test points or the associated SFI-5 interface.

Figure 8.9: Reference-cabling model for optical measurements



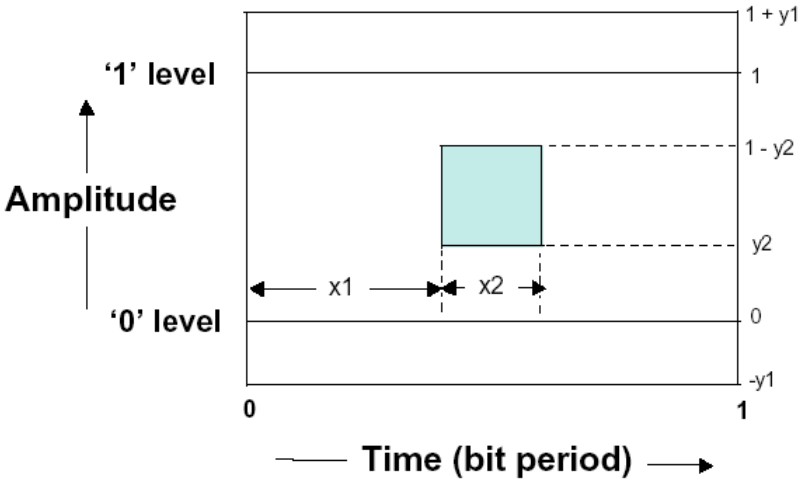
8.2.1.1 Transmitter Specification

The transmitters for the VSR link shall have 4 lasers multiplexed into 1 fiber of a SC duplex fiber cable assembly. Each laser shall individually meet all the specifications listed in Table 8.3. Furthermore, all elements in the transmitter for the VSR link shall also meet a transmit eye mask measurement as discussed in Section 8.2.3.

Table 8.3: Transmitter Characteristics

Parameter[20,21]	**Min.**	**Typ.**	**Max**	**Units**
Data rate	10.264 -11.09			Gb/s
Wavelength range	1269.0		1355.9	nm
Center wavelength - Channel 1	1269.0		1282.4	nm
Center wavelength - Channel 2	1293.5		1306.9	nm
Center wavelength - Channel 3	1318.0		1331.4	nm
Center wavelength - Channel 4	1342.5		1355.9	nm
$\Delta\lambda_{rms}$			0.62	nm
T_{rise}/T_{fall} (20-80%)			45	ps
RIN			-132.5	dB/Hz
Average Launch Power, four lanes			5.5	dBm
Average Launch Power, per lane	-5.5		-0.5	dB
Total Link Reflection			-12	dB
Transmitter Reflectance			-12	dB
Extinction Ratio[22]	6.0			dB
Average Launch Power of OFF transmitter, per lane			-30	dBm

Figure 8.10: Filtered and Unfiltered Eye Mask



	Filtered	Unfiltered
Y1	0.25	NA
Y2	0.25	0.40
X1	0.40	0.40
X2	0.20	0.20

[20] All specifications are per channel and at the end of a 2m patchcord.

[21] In the event of accidental transmitter to transmitter connection, no damage shall occur that will prevent the continued operation of the transmitter module within specification.

[22] Extinction Ratio is measured using the unfiltered eye mask in Figure 8.10.

An unfiltered eye specification is defined as the eye mask condition when the 4th order Bessel-Thomson filter is excluded from the measurement chain used in measuring the performance of the transmitter. When the filter is not used in the measurement, the chain consists of an O/E converter and a scope (or digital communications analyzer). In this case, an O/E converter with a bandwidth of at least 2.7x that of the measured data rate is specified for use in the measurement chain.

8.2.1.2 Receiver Specification

The receivers for the VSR link shall have 4 receiving elements multiplexed into a separate fiber in a SC duplex fiber cable assembly. Each receiving element shall individually meet all the specifications listed in Table 8.4.

The receiver shall have a minimum roll-off of 20 dB per decade to filter out the transmitter high frequency noise.

Table 8.4: Receiver Characteristics

Receiver[23,24]	**Min**	**Max**	**Units**
Data rate	10.264 -11.09		Gb/s
Wavelength range	1269.0	1355.9	
Center wavelength - Channel 1	1269.0	1282.4	
Center wavelength - Channel 2	1293.5	1306.9	
Center wavelength - Channel 3	1318.0	1331.4	
Center wavelength - Channel 4	1342.5	1355.9	
Average Receive Power four lanes		5.5	dBm
Average Receive Power per lane[25]	-12.0	-0.5	dBm
Wavelength range	1269.5	1355.9	nm
Receive electrical 3 dB upper cutoff frequency, per lane		13.2	GHz
Total Link Reflection[26]		-12	dB
Receiver Reflectance		-12	dB
Stressed receive sensitivity, per lane[27]	-9.58		dBm

[23] All receiver specifications are per channel.

[24] Receiver sensitivity shall be such that the BER ≤ 10^{-12} with the minimum optical power, worst case extinction ratio including the optical path penalty (includes 2.0dB loss for connectors), and the maximum crosstalk possibility.

[25] Each wavelength channel coming into the receiver is independent in power level. A maximum difference of 5dB in power is allowed between channels. Because of the optical separation of the signals, there are no other power constraints in how these channels inter-relate at the receiver.

[26] The return loss accounts for the whole link reflectance, including fiber interface reflections.

8.2.1.3 Link Power Budget and Penalties

The specifications in this section are based on a per channel data rate of 10.264-11.09Gb/s, with a maximum guaranteed link distance of 2000m. Calculation of optical link performance was conducted with Appendix 10.3 and the values given in Table 8.3 and Table 8.4.

Table 8.5: Link power budget and penalties for worst case link parameters

Description	Value				Units
Reference Application	Ref App 1	Ref App2	Ref App 3	Ref App 4	
Fiber Type	G.652	G.652	G.652	G.652	
Fiber modal BW	SMF	SMF	SMF	SMF	
Operating distance	2-100	2-300	2-600	2-2000	meters
Connector loss budget	2.0	2.0	2.0	2.0	dB
Link power budget	6.5	6.5	6.5	6.5	dB
Channel insertion loss	0.04	0.12	0.25	0.83	dB
Link power penalties	3.5	3.5	3.5	3.6	dB
Unallocated margin[28]	2.96	0.88	0.75	.07	dB

The maximum differential skew between optical channels over the length of the single mode fiber will be 3.5ps/m. Table 8.6 provides the worst-case skew budget (Reference Application 4).

Table 8.6: Skew Budget

Link Element	Skew Contribution
Transmitter	20 UI
Medium	80 UI
Receiver	20 UI
Total Skew[29]	120 UI

[27] The stressed sensitivity is specified to ensure receiver operation when maximum ISI and jitter is present. This parameter is informative.
[28] Unallocated margin is reserved for system vendor use.
[29] 100UI is the max skew permitted at the optical input to the receiver.

8.2.1.4 Jitter Specification

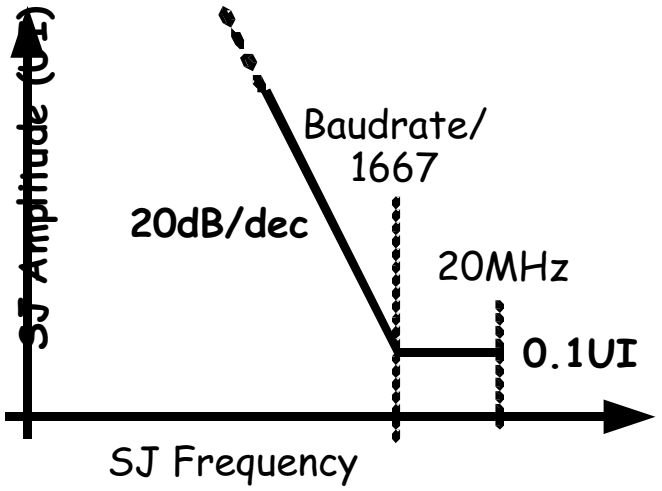
The jitter specification for the VSR link shall meet the same jitter specification as in the GBE specification [5, Sec. 38.5]. Jitter values for the model link shown in Figure 8.9 are given in Table 8.7. Note that the TP2 in the Gigabit Ethernet specification [5, 38.2.1] is equivalent to Point #1 in Figure 2, and TP3 in the Gigabit Ethernet specification [5, 38.2.1] is equivalent to Point #4 in Figure 3. Implementations shall conform to the normative values highlighted in bold; other values are informative.

Table 8.7: Jitter specification for link shown in Figure 8.9[30,31]

Compliance Point	Total Jitter[32]		Deterministic Jitter	
	UI	ps	UI	ps
Point #1	**0.431**	**39**	**0.200**	**18**
Point #1 to Point #2	0.170	15	0.050	5
Point #2	**0.510**	**46**	**0.250**	**23**

The receiver should be able to withstand wander as per Figure 8.11. (SJ refers to Sinusoidal Jitter), in the presence of high frequency jitter, where the total high frequency jitter does not exceed the total jitter defined for TP3.

Figure 8.11: Sinusoidal Jitter allowable amplitude vs. frequency



[30] Measured using a recovered clock that is filtered with a single pole high pass filter with a corner frequency of baudRate/1667.

[31] RJ is calculated as being the difference between total jitter and deterministic jitter. RJ is allowed to be increased given a smaller DJ.

[32] Total jitter is composed deterministic and random components. The allowed random jitter equals the allowed total jitter minus the actual deterministic jitter at that point.

8.2.2 Optical Fiber and Connector Specification

The fiber optic cable shall contain 2 fibers. The fiber in this implementation is specified as G.652 single mode fiber.

The maximum connector loss shall be 0.5dB per mating.

The externally accessible transmit and receive optical connectors shall be male connectors.

8.2.3 Measurement of the Optical Parameters

All measurement of the optical parameters shall be made through a 2m optical patch cable.[33] The recommendation of specific test patterns is provided in an effort to meet the overall objective of ensuring compliance of the standard under all valid data patterns.

For single channel measurement of optical parameters, the reference filter defined in section 8.2.3.9 will be utilized. This filter shall be utilized as needed for measurements defined in sections 8.2.3.1 - 8.2.3.8

8.2.3.1 Center Wavelength and Spectral Width

The center wavelength and spectral width shall be measured per EIA/TIA-455-127 using a PRBS31 from the converter or an external source input to the SFI-5 interface.

8.2.3.2 Optical power measurements

The optical power shall be measured as in [5, Sec. 38.6.2.] The measurement shall be made per EIA/TIA-455-95A using the pattern described in Section 8.2.3.1.

8.2.3.3 Extinction Ratio Measurements

The extinction ratio shall be measured as in [5, Sec. 38.6.3] This measurement may be made per EIA/TIA-526-4A using a square pattern consisting of four to eleven ones followed by an equal run of zeros.

[33] Where tests specify a Bessel -Thompson filter, the parameters of the filter need to be modified to reflect the increased data rate.

8.2.3.4 Eye Mask Test

In order to ensure interoperability among vendor components and systems, an eye mask test shall be performed. The filtered eye mask test shall be measured as in [5, Sec. 38.6.5] using the pattern described in Section 8.2.3.1.

8.2.3.5 Transmitter Rise/Fall Characteristics

The transmit rise/fall characteristics shall be measured as [5, Sec. 38.6.6] using the square pattern described in Section 8.2.3.3.

8.2.3.6 Receiver Sensitivity Measurements

Receivers shall be tested for sensitivity in conformance with [5, Sec. 38.6.7] Additionally there is a crosstalk requirement for the testing.

The receiver shall meet the required sensitivity specification with the required conformance test signal with the worst case crosstalk condition of maximum optical power received by the 2 adjacent channels.

The adjacent channels shall meet all the specifications in Table 8.3 and Table 8.4.

8.2.3.7 Receiver 3dB electrical upper cutoff frequency

The receiver 3dB electrical upper cutoff frequency shall be measured as [5, Sec. 38.6.12].

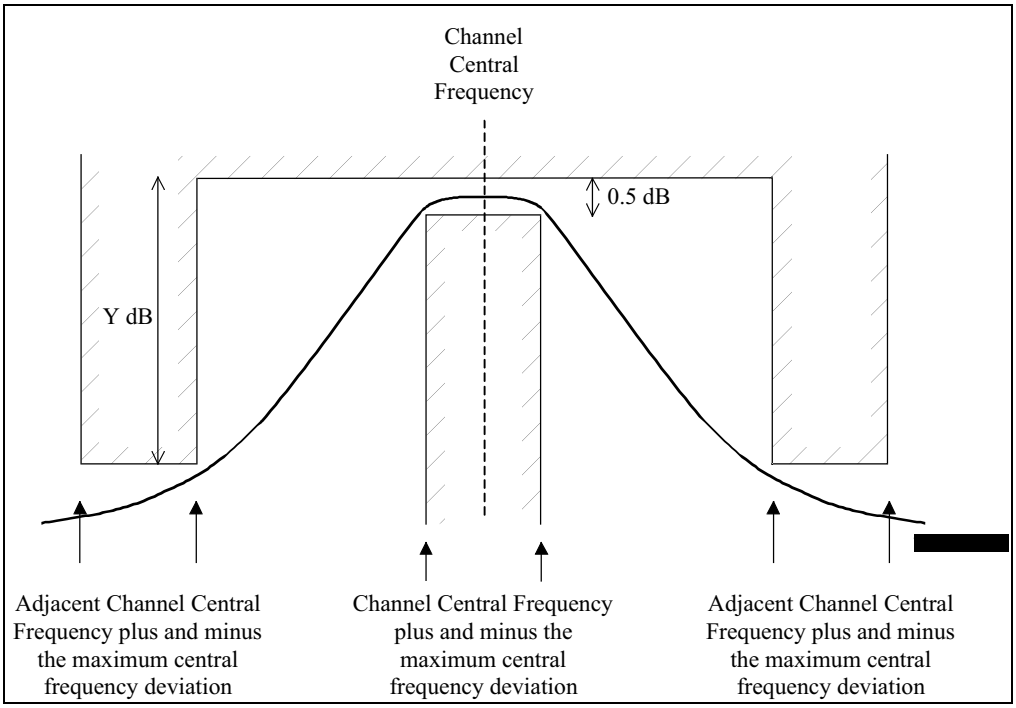
8.2.3.8 Jitter measurements

The jitter measurements shall be measured as in [5, Sec. 38.6.8 and 38.6.9].

8.2.3.9 Optical filter parameters

Referencing ITU document G.959.1 Section B.1, the requirements on the reference optical CWDM bandpass filter frequency response are illustrated in Figure 8.10. The value of Y is chosen such that the ratio of the power in the channel being measured to the sum of the powers of all of the other channels is greater than 20 dB.

Figure 8.12: Optical bandpass filter frequency response

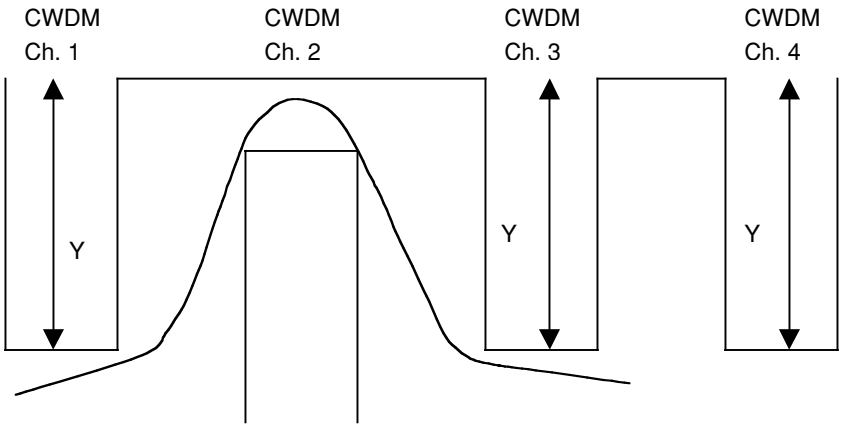


The design of the filter should be chosen so that a maximum rate signal should undergo no significant distortion due to amplitude and phase ripple.

In the case of the 4x10G CWDM solution figure 8.11 illustrates the four CWDM channels and the filter Y values required to meet the 20dB condition. The Ys are measured in dB such that the following condition must be met when measuring a specific CWDM channel:

$$\frac{\text{Power of Measured Channel}}{\text{Sum of power in remaining 3 CWDM Channels}} \Rightarrow 20\text{dB}$$

Figure 8.13: Four-channel CWDM filter requirements.



This condition holds for all four CWDM channel filters.

Table 8.8: CWDM Section Normative/Informative Matrix

Paragraph	Topic	Normative/Informative
Section 8 Intro	Introduction to 4x10G	Normative
8.1.1	Converter	Normative
8.1.2	Transmitter Block Functionality	Normative
8.1.2.1	Data Recovery and SFI-5 deskew	Normative
8.1.2.2	Data Framing	Normative
8.1.2.3	VSR-5 Four-channel data striping with 64b/66b	Normative
8.1.2.4	PRBS Generator	Informative
8.1.2.5	High speed data transmission	Informative
8.1.3	Receiver Block	Normative
8.1.3.1	Clock/Data Recovery	Normative
8.1.3.2	Frame Alignment and Deskew, first paragraph and Figure 8.6	Normative
8.1.3.2	Frame Alignment and Deskew, third and subsequent paragraphs	Informative
8.1.3.3	Scrambler	Normative
8.1.3.4	Loss of Synchronization	Informative
8.1.3.5	RXS Status Output	Normative
8.1.3.6	PRBS Checker	Informative
8.1.3.7	RXDCK output	Informative
8.1.3.8	RXDSC Channel Generation	Normative
8.1.4	Internal Register Block	Informative
8.1.5	Loopback Modes	Informative
8.1.6	SFI-5 Electrical Characteristics	Informative
8.1.7	Test Requirements	Informative
8.2	Optical Interface Specifications	Normative
8.2.1	Optical Reference points	Normative
8.2.1.1	Transmitter specifications	Normative
8.2.1.2	Receiver Specifications	Normative
8.2.1.3	Link Budget Specifications	Normative
8.2.1.4	Jitter Specifications	Normative
8.2.2	Optical Fiber and Connector Specification	Normative
8.2.3	Measurement of Optical Parameters	Normative

9 SERIAL SOLUTION

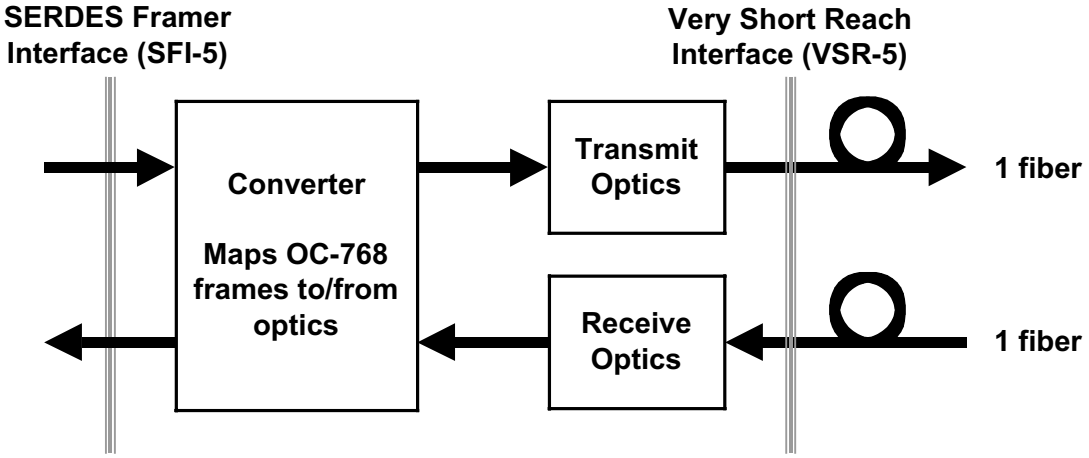
This 40G VSR interface uses serial optics to provide a solution for all the reference models as specified in Section 6. This serial option of VSR-5 is specified to be compatible with both SONET/SDH data format and G.709 Digital Wrapper. Whilst the OIF project specifically requires VSR-5 to transfer SONET/SDH data, G.709 Digital Wrapper data is included in the serial option to provide broader market acceptability.

Optical budgets are referenced to ITU-T G.693[10]. Solutions are specified employing both 1310 and 1550 optics. In order to provide solutions for all the specified OIF reference models, optical parameters are referenced for both 4dB and 12dB maximum link attenuation. The 4dB budget is compatible with link reaches up to 2 km, without a crossconnect, i.e. models 1 – 4. The 12dB budget is compatible with transmission through a photonic crossconnect, i.e. reference application number five. Note that for the interfaces having 12 dB maximum attenuation, G.693 calls for a minimum attenuation of 8 dB at 1310 nm, and 3 dB at 1550 nm. While these figures are higher than the 0 dB minimum attenuation called for in Reference Model 5, G.693 indicates that the latter is not believed to be achievable in the near future. Thus, while undesirable, the 0 dB minimum attenuation called for in Model 5 can only be achieved by using an optical attenuator in the path. Presumably, G.693 will be subject to amendment to address this when technology permits.

The 1310 optical specifications are compatible with transmission through standard (G.652) single mode duplex fibre. The 1550 specifications are further compatible with G.653 and G.655 fibre. All specifications describe an optical source and receiver capable of function over the 40G data rate range, including both SONET/SDH data at 39.813Gb/s and G.709 data at 43.018Gb/s (and considering the 20ppm rate tolerance).

The interface is bi-directional, with a single transponder element at each end of the fibre pair. A functional block diagram of a transponder is shown in Figure 9.1 below.

Figure 9.1: Functional block diagram of serial interface.



The VSR interface is considered as being terminated at the SFI-5 electrical interface of each transponder at each end of the fibre. OC-768/G.709 data is input to and output from the transponder via the SFI-5 interface. A converter IC within the transponder performs the function of converting from the 16 bit electrical SFI-5 interface to 40Gbit transmit and receive serial streams. It is likely that this converter function will be partitioned into multiple IC's, to take advantage of the performance of different technologies. The transponder also converts between serial electrical signals and optical data. Transmit and receive optics are included within the transponder.

A management interface is provided to communicate information such as alarms, optical parameters and to be able to configure the transponder into different test modes. Detail of this interface is not a subject of this document.

The SERDES -Framer Interface shown in the block diagram is compliant with the OIF SFI-5 Implementation Agreement, but limited to SONET/SDH and G.709 nominal data rates of 2.488 and 2.688 Gb/s.

In the transmit direction, the converter IC(s) multiplexes the 16bit parallel data into a serial electrical data stream. The mapping from the 16bit word to serial stream is described in section 5.1. The serial electrical signal interfaces to a modulator driver to source the 40Gbit NRZ optical data.

In the receive direction, the optical receiver converts from optical data to a serial electrical signal, which is amplified in order to interface internally to the converter IC(s). The Converter IC(s) demultiplexes the serial signal to a 16bit wide word. The mapping of the serial signal to 16bit wide word is described in Section 9.1.1.

9.1 Converter

The converter performs the function of multiplexing and demultiplexing from the 16bit SFI-5 interface to serial electrical data streams interfacing to the optical transmit and receive blocks.

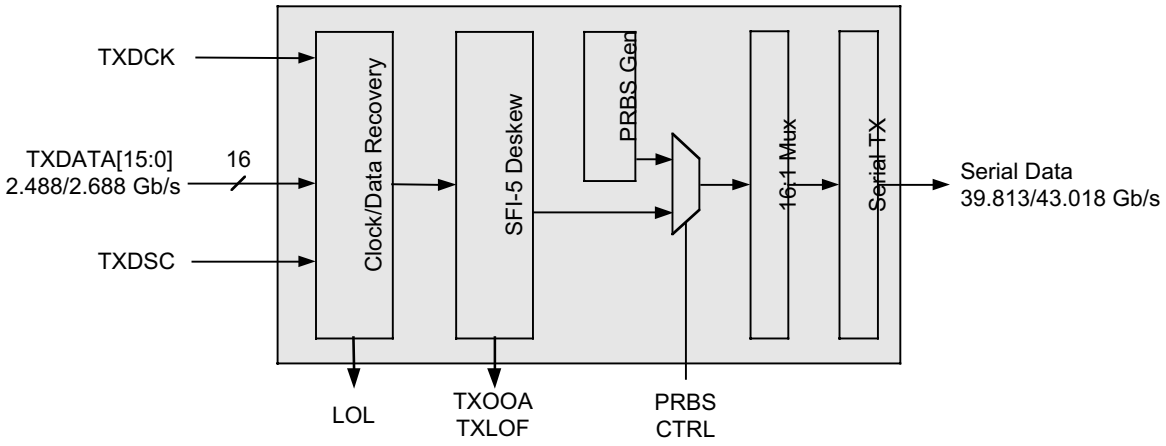
9.1.1 Transmiter Function

The transmitter section of the converter receives the 16 bit parallel data from the SFI-5 interface block. The SFI-5 block performs the clock/data recovery and deskew function, to compensate for skew in the parallel interface between the Framer and SERDES IC's, including the transponder connector. The transmitter provides a simple multiplex function to convert the parallel data to a serial stream. There is no recognition of byte or frame boundaries. Data on the parallel transmit bus TXDATA[15:0] is transferred to the serial stream in a round-robin fashion. TXDATA[15] contains the first bit to be transmitted, while TXDATA[0] contains the last bit to be transmitted.

The multiplexer function usually includes a clock synthesis PLL, which generates a low jitter clock from an external reference. This clock provides the jitter reference for the serial data stream, as well as providing clock to the multiplex function.

The transmit section of the converter also has the function of being able to multiplex in a PRBS test pattern for testing the optical output. This test function is controlled by the management interface and is shown in the block diagram in Figure 9.2.

Figure 9.2: Converter Transmit functional blocks



9.1.1.1 Data Recovery and SFI-5 Deskew

The SFI-5 interface block recovers data on each of TXDATA[15:0] and TXDSC at 2.488 – 2.688 Gb/s per channel as described in the SFI-5 Implementation Agreement. Although SFI-5 specifies that terminating devices must operate at data rates from 2.488 Gb/s to 2.7725 Gb/s, the VSR Converter is only required to accommodate a 2.488 – 2.688 Gb/s rate on its SFI-5 interface.

Data recovered on TXDATA[15:0] have up to the maximum amount of relative skew between them as is allowed by the SFI-5 specification. Data on the latest channel may lag data on the earliest channel by up to the specified number of UI. Bit lane deskew is accomplished with the TXDSC channel. TXDSC is a reference channel containing replicated data from each of the 16 data channels in a frame format described in the SFI-5 Implementation Agreement. The SFI-5 Interface and Deskew blocks contain the buffers, deskew controllers and delay elements necessary for lane-to-lane data deskewing. By comparing the data on each channel with its corresponding data on TXDSC, the skew between data and reference channel is deduced. Once the delay is known the delay element associated with that channel is adjusted for alignment between the data and reference channel. This is carried out on each channel successively until all data channels are deskewed relative to the reference channel and therefore relative to each other.

An out-of-alignment alarm TXOOA is set if pattern matching cannot be achieved on all 16 channels, and is cleared when it is achieved. After successfully deskewing the 16 channels, the skew on each channel is continuously monitored, allowing the Converter to track skew changes of up to the maximum amount allowed in the SFI-5 Implementation Agreement without introducing errors. A set of counters in the IRB is allocated for counting the instances of pattern mismatch between each channel's data and the corresponding data on the deskew channel. The SFI-5 IA contains greater detail on the deskewing algorithm and TXDSC frame format.

9.1.1.2 PRBS Generator

The transmitter contains a PRBS generator capable of generating a 2^{31}-1 serial PRBS pattern as required for system and chip level testing. The use and function of the PRBS generator are controlled through the IRB. The generating polynomial used for the PRBS 2^{31}-1 pattern is $x^{31} + x^{28} + 1 = 0$ with an inverted output.

9.1.2 Receive Function

The receive section of the converter receives a serial data stream from the optical detector and amplifier. It analyses the quality of the received signal, and generates the RXS status channel. The receive block normally includes a clock recovery function, which recovers a 40GHz clock from the NRZ data. This clock is used to clock the Demultiplex function and is transmitted upstream over the SFI-5 interface.

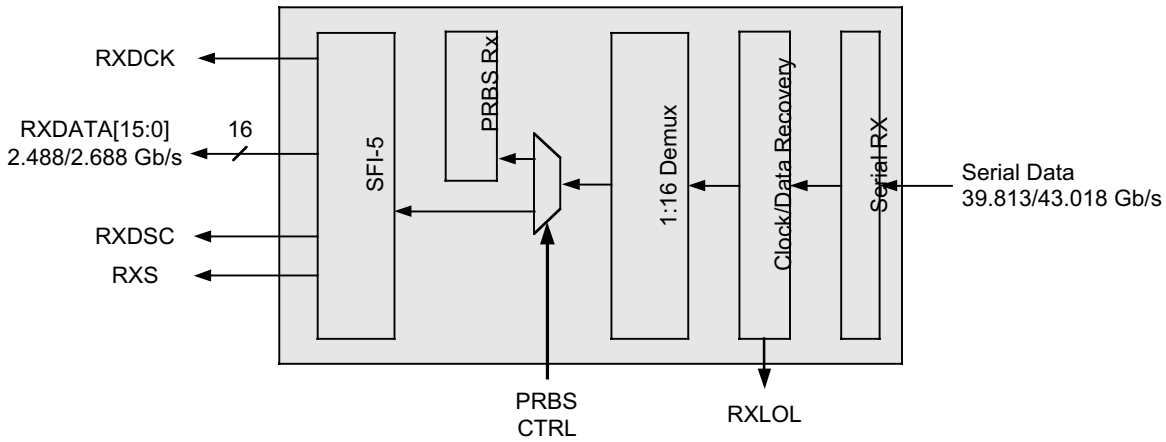
The receive function demultiplexes the serial data stream to 16 bit wide words, and outputs the 16 bit wide data over the SFI-5 interface. There is no requirement to identify byte or frame boundaries in the received data stream. Serial data is striped onto RXDATA[15:0] in a simple round robin fashion. RXDATA[15] contains the first bit received, while RXDATA[0] contains the last bit received. RXDATA[15:0] has arbitrary alignment to the bytes in the receive optical data stream.

The SFI-5 interface block generates the deskew channel RXDSC for transmission over the SFI-5 interface. This signal includes frame and header bytes, and copies of each of the 16 parallel channels, to enable deskew at the sink end of the SFI-5 interface. The SFI-5 IA contains greater detail description of the RXDSC deskew channel format.

The receive section of the converter also contains the function to test a received PRBS test signal. This function is controlled by the management interface.

The basic function of the Receive section is illustrated in Figure 9.3 below.

Figure 9.3: Converter Receive functional blocks



9.1.2.1 Loss of Received Clock

The Converter IC includes functionality to ensure that a continuous Receive data clock (RXDCK) is sent to the FEC processor or framer device. The optical receiver lock range will exceed 100ppm over temperature and supply range. The clock recovered from the received optical signal is compared with a clock derived from a reference frequency. If the recovered clock deviates from the reference frequency by more that 1000ppm, then RXDCK will switch from being sourced from the recovered clock to the reference clock (RXREFCK). Somewhere between 100ppm and 1000ppm, an out-of lock condition will be declared, and RXDCK shall switch from being sourced from the recovered clock to being sourced from the reference.

If loss of received data (LOS) is detected, then the RXDCK is sourced from the reference clock (RXREFCK).

Under conditions above when the RXDCK is not sourced from the received data, then the receive status alarm (RXS) will be set high.

Switching the receive data clock (RXDCK) shall be done such that the minimum pulse width and minimum period of RXDCK are not violated.

9.1.2.2 PRBS Checker

A PRBS checker that can be used to synchronize to and detect bit errors and synchronization errors in the serial PRBS data stream initiated in the transmitter section of a Converter is included. Errors are accumulated in IRB counters.

9.2 Optical Interface Specifications

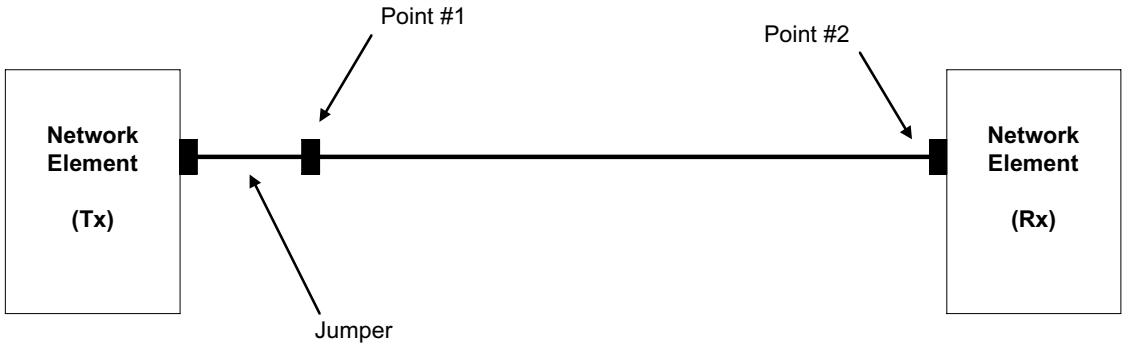
The optical interface specifications are defined in Table 9.1 below, referencing the ITU-T G.693 specification for VSR links. Optical link budgets are referenced for both 1310 and 1550nm optical sources. Links with a max path attenuation of 4dB are compatible with reference models 1 – 4, i.e. up to reach of 2km. Links with max path attenuation of 12dB are compatible with reference model no 5, i.e. with reach up to 600m through a photonic crossconnect. Although reference model 5 defines optical reach only up to 600m, the ITU model specifies reach up to 2km.

The data format for all links is 40G NRZ. Data rate is compatible with both SONET/SDH at 39.813GB/s and G.709 digital wrapper at 43.018Gb/s.

9.2.1 Optical Specification Reference Points

Measurements of the transmitter (Tx) and receiver (Rx) optical parameters are made at Point #1 and Point #2 respectively of the reference-cabling model illustrated in Figure 9.4 below. Point #1 corresponds to MPI-S in the ITU spec, point #2 corresponds to MPI-R in the ITU spec.

Figure 9.4: Reference-cabling model for optical measurements



9.2.2 Optical Specifications

The ITU-T application codes referenced below in Table 9.1 define the Optical Transmit and Receive parameters, and specification of the optical path.

Table 9.1: Optical parametric specification references.

Link attenuation range	**0 to 4dB**	**0 to 4dB**	**8[34] to 12dB**	**3[14] to 12dB**
Nominal Operating wavelength	**1310nm**	**1550nm**	**1310nm**	**1550nm**
ITU-T Application code	VSR2000-3R1	VSR2000-3R2 VSR2000-3R3 VSR2000-3R5	VSR2000-3M1	VSR2000-3M2 VSR2000-3M3 VSR2000-3M5
OIF Application reference models	1, 2, 3, 4	1, 2, 3, 4	5	5
Fibre Type	G.652	G.652 G.653 G.655	G.652	G.652 G.653 G.655

[34] According to G.693, “This value of minimum attenuation is highly undesirable. A value of 0 dB is desired and should be sought as technology matures.” To fully satisfy reference model 5, attenuators may be required in the optical path.

9.2.3 Jitter Specifications

Jitter specifications for each of the 4dB and the 12dB links are as specified by the ITU in G.783 for SONET/SDH and G.8251 for G.709.

9.2.4 Eye Pattern Masks

The transmitted pulse shape for each the 4 dB and 12 dB links are as specified by the ITU in G.693.

Table 9.2: Serial Section Normative/Informative Matrix

Paragraph	Topic	Normative/Informative
9.1	Converter	Normative
9.1.1	Transmiter Function	Normative
9.1.1.1	Data Recovery and SFI-5 Deskew	Normative
9.1.1.2	PRBS Generator	Informative
9.1.2	Receive Function	Normative
9.1.2.1	Loss of Received Clock	Informative
9.1.2.2	PRBS Checker	Informative
9.2	Optical Interface Specifications	Normative
9.2.1	Optical Specification Reference Points	Normative
9.2.2	Optical Specifications	Normative
9.2.3	Jitter Specifications	Normative
9.2.4	Eye Pattern Masks	Normative

10 INFORMATIVE APPENDICES

This informative appendix is only for information and guidance. These 10 Gigabit Ethernet spreadsheets were used to determine optical parameters for the 12 channel and CWDM sections of this document.

10.1 10 GE Power Budget Spreadsheet for 12 Channel 500 MHz.km fiber

Spreadsheet by Del Hanson, David Cunningham, Piers Dawe, David Dolfi Agilent Technologies | Rev. 3.2/3 | This file 10GEPBud3_1_16.xls of 17-Oct-01 | Model/format rev 3.1.16 of 16-Oct-01

Basics
Input= Bold
Q= 7.04
Base Rate= 3317.76 MBd

Transmitter
Wavelength Uc 830 nm
Uw (see notes) 0.65 nm
Tx pwr OMA= -7.22 dBm
Min. Ext Ratio= 6.00 dB
"Worst"ave.TxPwr -8.0 dBm
Ext. ratio penalty 2.23 dBo
Tx mask X1= 0.4 UI
X2= 0.4 UI
Y1= 0.25

Ts(20-80) 120 ps
Ts(10-90) 182 ps
RIN(OMA) -119.5 dB/Hz
RIN at MinER -124.0 dB/Hz
RIN_Coef= 0.70
Det.Jitter 30.1 ps inc. DCD
DCD_DJ= 30.1 ps TP3
Effect. DJ= 0.00 (UI) ex DCD
MPN k(OMA) 0.3
Tx eye height 57.8%
Refl Tx -12 dB
ModalNoisePen 0.3 dB
Tx mask top 0.2 UI

Case: 850nm serial 50MMF
Target Target reach 0.160 km
and L_start= 0.05 km
graph L_inc= 0.01 km
Power Budget P= 7.00 dB
Connections etc 0 dB
Pwr.Bud.-Conn.Loss 7 dB
C1= 480 ns.MHz
Reflection Noise factor 0 no units
Effective Rate 3686 MBd
Tb_eff= 271 ps
Effective Rec Eye 0.22 UI

Attenuation= 3.5 dB/km
Fiber at 850 nm
C_att= 1.00
Attenuation= 3.75 dB/km
at 830 nm
Disp. min. Uo= 1320 nm
Disp. So= 0.11 ps/nm^2*km
Disp. D1= -123.19 ps/(nm.km)
(not in use) 10
BWm= 350 MHz*km
Eff. BWm= 3.5E+02 MHz*km

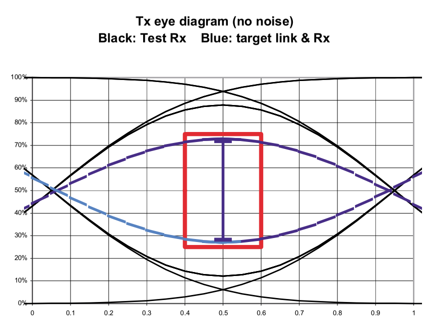
NomSens OMA -14.22 dBm
Receiver Refl Rx -12 dB
Rec_BW= 2,500 MHz
c_rx 329 ns.MHz
T_rx(10-90) 131.6 ps
TP4 Eye 60 ps
Opening (=Tx ey
RMS Baseline wander SD 0.025 fraction of 1/2 eye
P_BLW(no ISI) 0.07 dB
P_BLW 0.07 dB

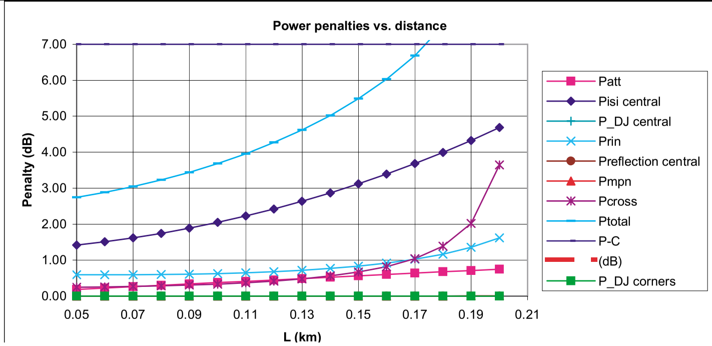
Margin 0.97 dB at
Answer! 0.16 km
Test Rx BW 2500 MHz
Test Source ER=
Test Tx 6.5 dB
TestERpen 1.98 dBo
V.E.C.P. 3.39 dBo
Stressed Rx sens

L (km)	Patt (dB)	Ch IL (dB)	D1.L ps/nm	D2.L ps/nm	BWcd (MHz)	effBWm (MHz)	Te (ps)	Tc (ps)	Pisi central J=0, dB	P Eye corners (dB)	P_DJ central (dB)	P_DJ corners (dB)	Preflection central (dB)	Beta	SDmpn	Pmpn (dB)	Prin (dB)	Pcross central (dB)	Ptotal central (dB)	<Ptotal corners (dB)	LP Pen central (dB)	Margin (dB)	OMA central (dBm)
0.002	0.01	0.01	-0.25	0.00	1E+06	1.8E+05	182	225	1.21	0.26	0.00	0.00		-2E-03	0.00	0.00		0.08	1.60	1.86	1.6	5.40	-8.54
0.05	**0.19**	**0.19**	**-6.2**	**0.00**	**46,708**	**7,000**	**195**	**235**	**1.42**	**0.26**	**0.00**	**0.00**	**0**	**-0.05**	**0.00**	**0.00**	**0.60**	**0.24**	**2.7**	**3.0**	**2.6**	**4.25**	**-9.40**
0.06	0.22	0.22	-7.4	0.00	38,923	5,833	200	240	1.51	0.26	0.00	0.00	0	-0.06	0.00	0.00	0.59	0.25	2.9	3.1	2.7	4.12	-9.44
0.07	0.26	0.26	-8.6	0.00	33,363	5,000	206	245	1.62	0.27	0.00	0.00	0	-0.06	0.00	0.00	0.59	0.27	3.0	3.3	2.8	3.96	-9.48
0.08	0.30	0.30	-9.9	0.00	29,192	4,375	213	251	1.74	0.27	0.00	0.00	0	-0.07	0.00	0.00	0.60	0.28	3.2	3.5	2.9	3.77	-9.53
0.09	0.34	0.34	-11.1	0.00	25,949	3,889	221	257	1.89	0.27	0.00	0.00	0	-0.08	0.00	0.00	0.61	0.30	3.4	3.7	3.1	3.56	-9.59
0.10	**0.37**	**0.37**	**-12.3**	**0.01**	**23,354**	**3,500**	**229**	**264**	**2.05**	**0.27**	**0.00**	**0.00**	**0**	**-0.09**	**0.00**	**0.00**	**0.62**	**0.33**	**3.7**	**4.0**	**3.3**	**3.32**	**-9.66**
0.11	0.41	0.41	-13.6	0.01	21,231	3,182	238	272	2.23	0.27	0.00	0.00	0	-0.10	0.00	0.00	0.65	0.37	4.0	4.2	3.5	3.04	-9.74
0.12	0.45	0.45	-14.8	0.01	19,461	2,917	247	280	2.42	0.27	0.00	0.00	0	-0.11	0.00	0.00	0.68	0.42	4.3	4.5	3.8	2.73	-9.83
0.13	0.49	0.49	-16.0	0.01	17,964	2,692	256	288	2.64	0.27	0.00	0.00	0	-0.12	0.00	0.00	0.72	0.48	4.6	4.9	4.1	2.38	-9.94
0.14	0.52	0.52	-17.2	0.01	16,681	2,500	266	297	2.87	0.27	0.00	0.00	0	-0.13	0.00	0.00	0.77	0.56	5.0	5.3	4.5	1.98	-10.06
0.15	**0.56**	**0.56**	**-18.5**	**0.01**	**15,569**	**2,333**	**276**	**306**	**3.12**	**0.28**	**0.00**	**0.00**	**0**	**-0.14**	**0.00**	**0.00**	**0.83**	**0.67**	**5.5**	**5.8**	**4.9**	**1.51**	**-10.22**
0.16	0.60	0.60	-19.7	0.01	14,596	2,188	287	316	3.39	0.28	0.00	0.00	0	-0.15	0.00	0.00	0.92	0.82	6.0	6.3	5.4	0.97	-10.42
0.17	0.64	0.64	-20.9	0.01	13,738	2,059	298	326	3.68	0.28	0.00	0.00	0	-0.16	0.01	0.00	1.02	1.04	6.7	7.0	6.0	0.31	-10.68
0.18	0.67	0.67	-22.2	0.01	12,974	1,944	309	336	3.99	0.29	0.00	0.00	0	-0.17	0.01	0.00	1.17	1.39	7.5	7.8	6.9	-0.53	-11.03
0.19	0.71	0.71	-23.4	0.01	12,291	1,842	320	346	4.33	0.29	0.00	0.00	0	-0.18	0.01	0.00	1.36	2.02	8.7	9.0	8.0	-1.73	-11.58
0.20	**0.75**	**0.75**	**-24.6**	**0.01**	**11,677**	**1,750**	**332**	**357**	**4.69**	**0.30**	**0.00**	**0.00**	**0**	**-0.19**	**0.01**	**0.01**	**1.62**	**3.65**	**11.0**	**11.3**	**10.3**	**-4.01**	**-12.69**

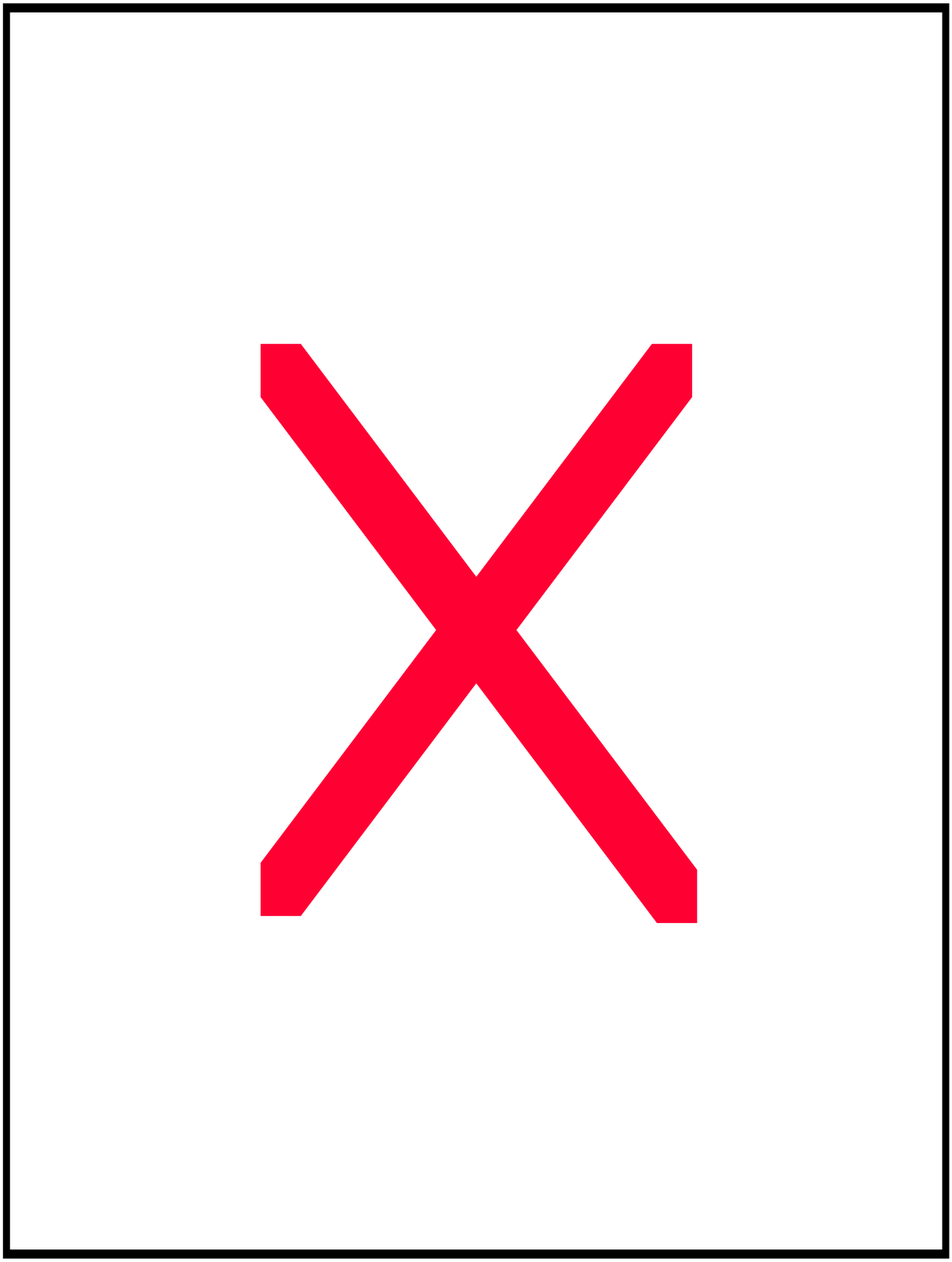
Notes **Draft**
See"Notes" page

To switch polarisation Mode Dispersion off, change box L2 from "SMF"

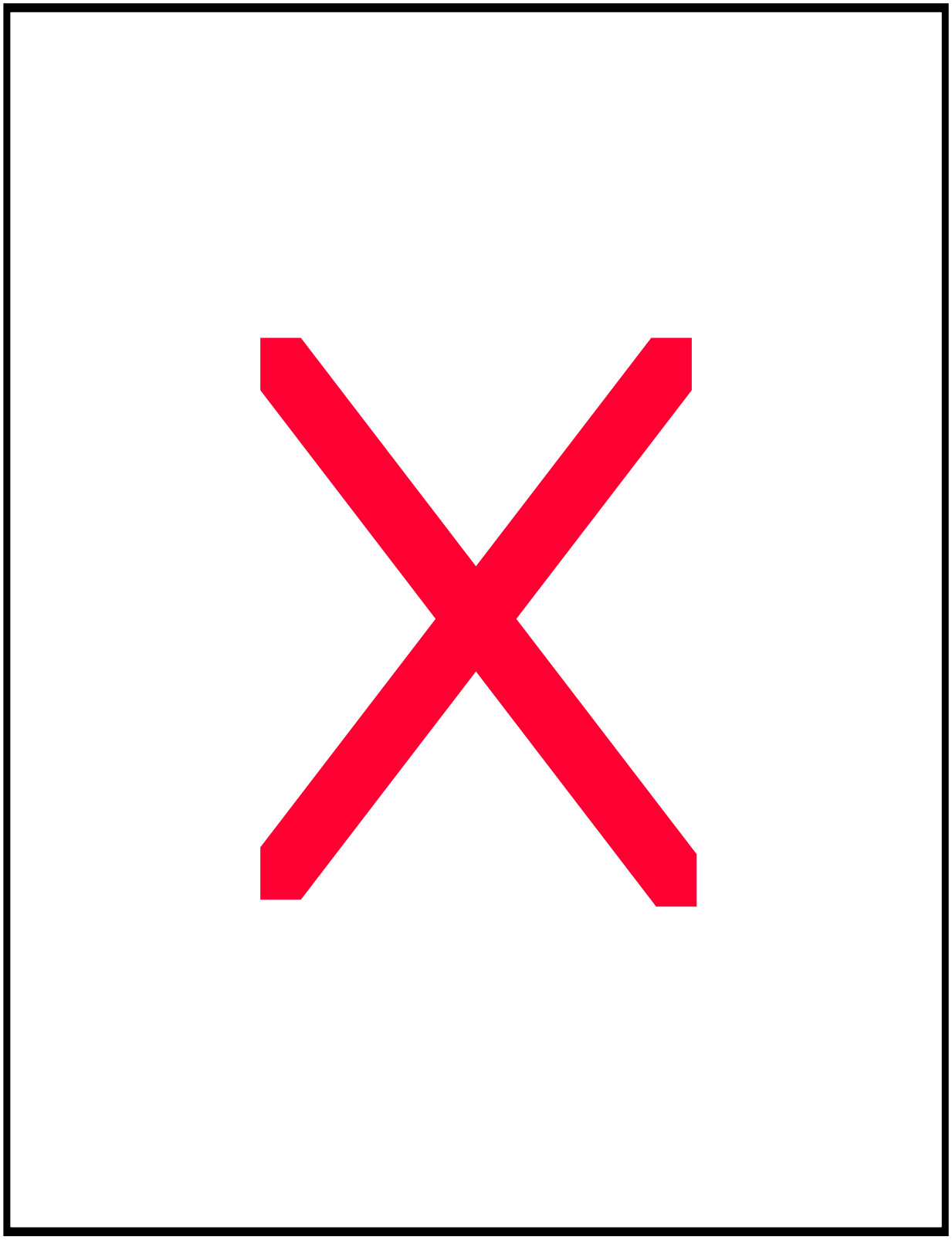




10.2 10 GE Power Budget Spreadsheet for 12 Channel 2000 MHz.km fiber



10.3 10 GE Power Budget Spreadsheet for Four Channel CWDM



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12 GLOSSARY

ADM	Add-drop Multiplexers
BIP	Bit Interleaved Parity
CID	Continuous Identical Digits
CML	Current Mode Logic
CWDM	Coarse Wavelength Division Multiplexing
DWDM	Dense Wavelength Division Multiplexers
GBE	Gigabit Ethernet
IA	Implementation Agreement
IRB	Internal Register Block
LOL	Loss of Lock
LOS	Loss of Signal
MMF	Multimode Fiber
MSB	Most Significant Bit
OIF	Optical Internetworking Forum
OOF	Out of Frame
PRBS	Pseudo-Random Bit Sequence
RIN	Relative Intensity Noise
SEF	Severely Errored Frame
SFI	SERDES Framer Interface
SJ	Sinusoidal Jitter
SMF	Single Mode Fiber
SONET	Synchronous Optical NETwork
VCSEL	Vertical Cavity Surface Emitting Laser
VSR	Very Short Reach

13 APPENDIX: LIST OF COMPANIES BELONGING TO OIF WHEN DOCUMENT IS APPROVED

Accelerant Networks
Accelight Networks
Actel
Acterna Eningen GmbH
ADC Telecommunications
Aeluros
Agere Systems
Agilent Technologies
Agility Communications
Alcatel
All Optical Networks, Inc.
Altamar Networks
Altera
Alvesta Corporation
AMCC
America Online
Ample Communications
Analog Devices
ANDO Corporation
Anritsu
Aralight
ASTRI
AT&T
Atrica Inc.
Avici Systems
Axiowave Networks
Bandwidth9
Bay Microsystems
Big Bear Networks
Bit Blitz Communications
Blaze Network Products
Blue Sky Research
Bookham Technology
Booz-Allen & Hamilton
Broadcom
Cable & Wireless
Cadence Design Systems
Calient Networks
Calix Networks
Caspian Networks
Celion Networks

Centellax
Centillium Communications
Ceyba
Chiaro Networks
Chunghwa Telecom Labs
Ciena Communications
Cisco Systems
Coherent Telecom
Conexant
CoreOptics
Coriolis Networks
Corrigent Systems
Cortina Systems
Corvis Corporation
Cypress Semiconductor
Data Connection
Department of Defense
DeriveIt
E2O Communications
ELEMATICS
Elisa Communications
Emcore
Equant Telecommunications SA
Equipe Communications
Ericsson
ETRI
Extreme Networks
EZChip Technologies
Fiberhome Telecommunications
Fiberspace
Finisar Corporation
Flextronics
Force 10 Networks
France Telecom
Free Electron Technology
Fujikura
Fujitsu
Furukawa Electric Technologies
Galazar Networks
General Dynamics
Glimmerglass Networks
Harris Corporation
Harting Electro-Optics GmbH
Helix AG
Hi/fn
Hitachi

Huawei Technologies
IBM Corporation
Ignis Optics
Industrial Technology Research Institute
Infineon Technologies
Infinera
Innovance Networks
Inphi
Integrated Device Technology
Intel
Internet Machines
Interoute
Intune Technologies, Ltd.
Iolon
Japan Telecom
JDS Uniphase
Jennic
Juniper Networks
KDDI R&D Laboratories
Kirana Networks
KT Corporation
Larscom
Lattice Semiconductor
LSI Logic
Lucent
Lumentis
LuxN
LYNX - Photonic Networks
Mahi Networks
Marconi Communications
MathStar
Maxim Integrated Products
MergeOptics GmbH
Meriton
Metro-OptiX
Mintera
Mitsubishi Electric Corporation
Multilink Technology Corporation
Multiplex
MultiWave Networks
Myrica Networks
Mysticom
National Semiconductor
Nayna Networks
NEC
NetTest

Network Elements
NIST
Nortel Networks
NTT Corporation
NurLogic Design
OpNext
Optical Datacom
Optillion
Optium
Optix Networks
Optobahn
OptronX
PacketLight Networks
Parama Networks
Paxonet Communications
Peta Switch Solutions
PhotonEx
Photuris, Inc.
Phyworks
Picarro
Pine Photonics Communications
PMC Sierra
Polaris Networks, Inc.
Princeton Optronics
Procket Networks
Quake Technologies
Qwest Communications
RedClover Networks
RF Micro Devices
RHK
Sandia National Laboratories
Santec Corporation
Santel Networks
Santur
SBC
Siemens
Sierra Monolithics
Silicon Access Networks
Silicon Labs
Silicon Logic Engineering
Sky Optix
Solidum
Southampton Photonics
Spirent Communications
StrataLight Communications
Stratos Lightwave

Sumitomo Electric Industries
Sun Microsystems
Sycamore Networks
TDK Semiconductor
Tektronix
Telcordia Technologies
Telecom Italia Lab
Tellabs
Tellium
Tenor Networks
TeraBurst Networks
TeraConnect
Teradiant Networks, Inc.
Texas Instruments
T-Networks, Inc.
Toshiba Corporation
Transpectrum
Transpera Networks
TriQuint Semiconductor
Tropic Networks Inc.
Tsunami Photonics
T-Systems Nova
Turin Networks
Tyco Electronics
US Conec
Velio Communications
Velocium (TRW)
Verizon
Vitesse Semiconductor
VSK Photonics
W.L. Gore & Associates
Wavecrest Corporation
Wavium AB
West Bay Semiconductor
Xanoptix
Xelerated
Xignal Technologies
Xilinx
Xindium
Xlight Photonics
Zagros Networks
Zarlink Semiconductor