TFI-5: TDM Fabric to Framer Interface Implementation Agreement

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ABSTRACT: This IA lists objectives for TFI-5 connects TDM fabrics to SONET/SDH and OTN Framers (TDM Fabric to Framer Interface or TFI-5), with line-side interface rates of up to OC-768, STM-256 or OTU-3. The interface supports synchronous time-division multiplexed switches that have a minimum granularity of STS-1 and above.

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4. Document Revision History

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oif2002. 287.16 29 July 2003 TFI-5 Implementation Agreement Draft 16, Updated appendix D labels.

oif2002. 287.17 6 August 2003 TFI-5 Implementation Agreement Draft 17, minor editorial changes.

5. References

[1] Optical Internetworking Forum, OIF2001.149.14, “SxI-5: Electrical Characteristics of Common I/O for SFI-5 and SPI-5”, November 2002.

[2] Optical Internetworking Forum, OIF-SFI5-01.0 - SerDes Framer Interface Level 5 (SFI-5): 40Gbps Interface for Physical Layer Devices.

[3] Optical Internetworking Forum, OIF-SPI5-01.1 - System Packet Interface Level 5 (SPI-5): OC-768 System Interface for Physical and Link Layer Devices.

[4] Telcordia, GR-253-CORE, Issue 3 Sept. 2000 – “Synchronous Optical Network (SONET) Transport System: Common Generic Criteria”

[5] ITU-T, Recommendation G.707, Oct. 2000 – "Network Node Interface For The Synchronous Digital Hierarchy (SDH)"

[6] ITU-T, Recommendation G.709, Feb. 2001 – “Network Node Interface for the Optical Transport Network (OTN)”

[7] ITU-T, Recommendation G.707, Amendment 2, 2002 – "Network Node Interface For The Synchronous Digital Hierarchy (SDH), Amendment 2"

[8] IEEE, 802.3ae-2002, “Information Technology - Local & Metropolitan Area Networks - Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications - Media Access Control Parameters, Physical Layers and Management Parameters for 10 Gb/s Operation”

[9] ANSI; T1.105, 2001; "Synchronous Optical Network (SONET) - Basic Description Including Multiplex Structure, Rates and Formats"

[10] IEEE standard 802.3ae-2002 (Amendment to IEEE Standard 802.3-2002)

6. Introduction

There are a number of vendors either offering or involved in offering TDM switching fabrics. Similarly, there are a number of vendors offering TDM framers, which interface to these switch fabrics. Traffic between the framer and the fabric is modeled after a SONET/SDH frame, and operates at the STS-48/STM-16 equivalent bit rate over the backplane. In order to ensure device interoperability across multiple vendor devices it is important that the electrical/optical jitter, and byte signaling protocols are compatible. This **T**DM Fabric to **F**ramer **I**nterface (TFI-5) Implementation Agreement is intended to ensure interoperability through the specification of key functions and/or parameters. The key functions specified within this document include link integrity monitoring, connection management, and mapping mechanisms for both SONET/SDH and non-SONET/SDH clients. TFI-5 is an alternative framer interface compared to SPI-5 [3], which is targeted for packet/cell switch fabrics.

At the August 2001 OIF Plenary meeting, a project was approved to generate an Implementation Agreement called TFI-5 (TDM Fabric to Framer Interface) to connect SONET/SDH framers to TDM fabrics using I/O technologies [1] developed for SFI-5 [2] and SPI-5 [3].

7. Requirements

The TFI-5 interface shall have the following requirements:

- Support SONET/SDH framers with line-side interfaces of OC-48/STM-16, OC-192/STM-64, and OC-768/STM-256.
- Support multi-channel framers with lower rate line-side interfaces with an aggregate bandwidth of N x OC-48/STM-16. (e.g. quad OC-12/STM-4).
- Support any standard compliant mix of non—concatenated, contiguously concatenated and virtually concatenated STS-1-SPE/higher order VC-3 and STS-3c-SPE/VC-4 payloads mapped within the above OC-Ns/STM-Ns.
- Support G.709 OTN framers with line-side interfaces of OTU1, OTU2, and OTU3 by mapping the ODU1, ODU2 and ODU3 into SONET/SDH-like frame formats.
- Support a line-side 10 GE WAN PHY interface as OC-192/STM-64 signal.
- Support for a line-side 10GE LAN PHY interface by mapping into a SONET/SDH-like frame format.
- Uses scrambling to ensure transition density.
- Support lane bandwidths of 2.488 Gbps and include a mechanism to support higher aggregate payload bandwidths across multiple lanes. All lanes are frequency locked to a common reference. Optionally, the TFI-5 link can also operate at a rate of 3.1104 Gbps (STS-60).
- Support byte interleaving.
- Supports de-skew between lanes originating from multiple framers or fabric devices. De-skew algorithm must operate without additional signal lanes.
- Support fabric constructed from multiple devices.
- TFI-5 device shall be capable of checking for errors.
- Capable of driving at least 30 inches of PCB with 2 connectors for intra-shelf environments and at least 100 meters over optics for inter-shelf environments.

- Capable of bit error rate of 10E-12 for PCB and for Optical links. Will have distance de-rating for better BER.
- Support DC coupling. AC coupling is optional.
- Provide a clear forward migration path to future fabrication processes.
- Wide availability of components.

8. Interface Definition

TFI-5 is a SONET/SDH-like backplane interface, either electrical or optical, connecting a framer to a TDM switch.

A system reference model is shown in Figure 8.1. A variety of framers, including SONET/SDH, OTN, 10GE WAN PHY and 10GE LAN PHY framers, are shown to operate simultaneously in the system. The transport of client signals through the TFI-5 system is fully specified, within the TFI-5 Implementation Agreement, for SONET and SDH signals (including the 10GE WAN PHY). The transport, through the TFI-5 system of OTN ODU1 and ODU2 clients are defined in Section 10.4. ODU3 and 10GE LAN PHY client mappings are proposed in Appendix A.

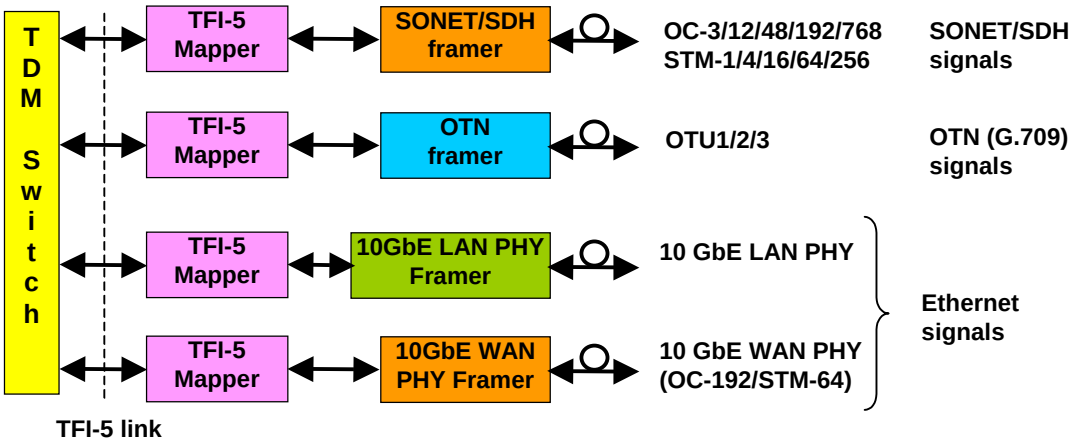


Figure 8.1 TFI-5 System Reference Model

As the services provided by the TFI-5 link in the Framer-to-Fabric direction, are identical to that provided in Fabric-to-Framer direction, there is only one definition of a TFI-5 link. It is applicable for either direction of traffic. Separate receive and transmit link definitions are unnecessary. All instantiations of the TFI-5 links in Figure 8.1 are identical: a 2.488 Gbps (or 3.1104 Gbps) link locked to a common system reference clock. The TFI-5 link has the following general characteristics:

1. A TFI-5 link is a point-to-point connection between a framer and a TDM switch fabric device.

2. The format of a TFI-5 link, the TFI-5 frame, is a simplification from Telcordia GR-253-CORE [4], ANSI T1.105 [9] and ITU G.707 [5] SONET/SDH frame (see Section 10). A1/A2 bytes are used for framing, the $X^7 + X^6 + 1$ scrambling polynomial is used to ensure rich transition

density, B1 is used for link error monitoring, and B2 can be used for connection monitoring.

3. TFI-5 is defined using a layered approach. Three different layers are defined (see Figure 10.4): Link layer, Connection layer and Mapping layer. The Link layer is generated and terminated by the TFI-5 link source and sink devices and its extent is a TFI-5 link. The Connection layer is generated/ terminated by the framer and its extent is the connection of a tributary (an STS-1 time-slot) from the Ingress framer to the Egress framer, passing through the TDM switch fabric. The Mapping layer is also generated/terminated by the framer. It provides the transport of client signals over one or more Connection layer time-slots.

4. All TFI-5 links are frequency locked and all theTFI-5 frames need to be relatively frame aligned within the deskew window of the fabric. Methods of aligning client signals to the TFI-5 frame include pointer processing and multiplexing/demultiplexing and/or through a mapping process.

The use of TFI-5 to connect a framer to a framer, or a TDM switch to a TDM switch, is out of the scope of the TFI-5 Implementation Agreement, but is not precluded.

9. Signal Definition

There are only three signals defined in TFI-5; a data signal (TFIDATA), a reference clock signal (TFIREFCK) and an 8kHz frame boundary reference (TFI8KREF). TFIREFCK and TFI8KREF shall be frequency locked to each other with a relative wander of less than +/- 4 UI of TFIREFCK. TFIDATA is differential CML. Examples of intra-shelf and inter-shelf system models are provided in Figures 9.1 and 9.2.

Signal Name	Function
TFIDATA	The **TFI-5 Data** (TFIDATA) signal carries the data between the Framer and the Switch Fabric. The same signal definition is applicable to data transfer in the Framer to Fabric direction, and the Fabric to Framer direction. Each TFIDATA link operates at 2.488 Gbps, corresponding to the standard SONET STS-48 rate and to the standard SDH STM-16 rate. Optionally, each TFIDATA link can operate at a rate of 3.1104 Gbps (STS-60), but support for the 3.1104 Gbps rate is not required. Each TFIDATA link transports TFI-5 frames (the frame format of TFIDATA). Each TFI-5 frame is modeled after a SONET / SDH stream. TFIDATA is frequency locked to TFIREFCK.
TFIREFCK	The **TFI-5 Reference Clock** (TFIREFCK) signal provides timing reference to all the TFI-5 data (TFIDATA) signals in a system. TFIREFCK is nominally a 155.52 MHz, 50% duty cycle clock. Jitter characteristics of TFIREFCK do not directly concern interoperability and are beyond the scope of this implementation agreement. All TFIDATA signals in a system are frequency locked to TFIREFCK.
TFI8KREF	The **TFI-5 8kHz Frame Reference** (TFI8KREF) signal provides reference to frame boundaries for all the devices in a TFI-5 system. TFI8KREF is nominally a 50% duty cycle clock with a nominal frequency of 8kHz. TFIREFCK and TFI8KREF shall be frequency locked to each other with a relative wander of less than +/- 4 UI of TFIREFCK.

Table 9.1 TFI-5 Signal Summary

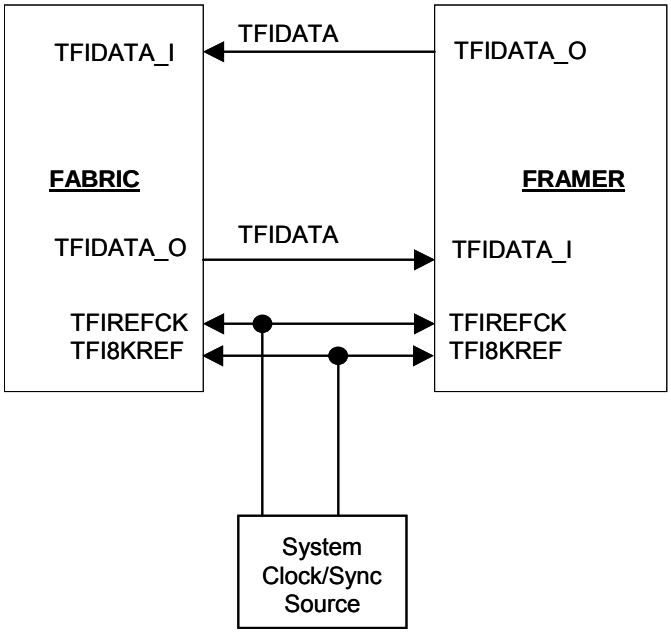


Figure 9.1 TFI-5 Intra-shelf system model

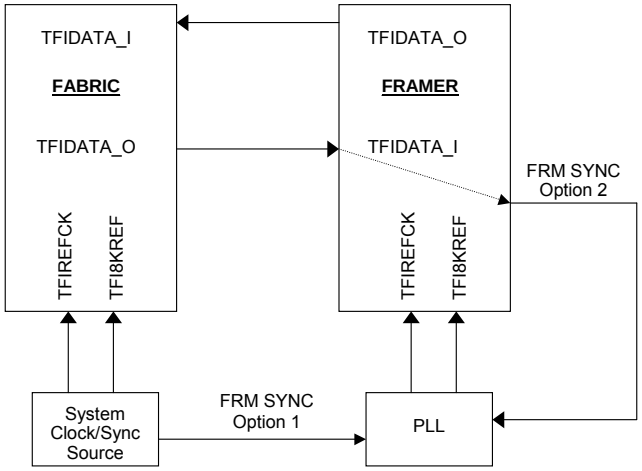


Figure 9.2 TFI-5 Inter-shelf system model with two example clocking implementations.

10. Detailed Description

TFI-5 is a SONET/SDH-based backplane interface, either electrical or optical, connecting a framer to a TDM switch fabric. TFI-5 uses a frame-based protocol. Figure 10.1 shows the format of a generic TFI-5 frame, where parameter N is the number of STS-1 time-slots (N = 48 or 60). The colors depicting bytes in figures 10.1, 10.2, and 10.3 correspond with the layers shown in figure 10.4.

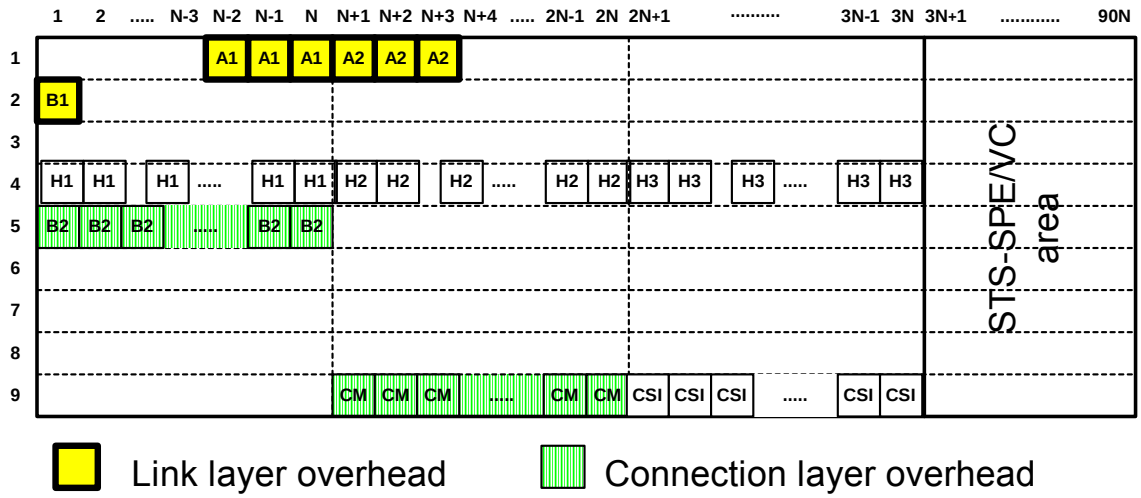


Figure 10.1 TFI-5 Frame Format (Generic)

Figure 10.2 shows the TFI-5 2.488 Gbps frame format (N = 48). This frame has the same dimensions as a standard SONET STS-48 or SDH STM-16 frame (9 rows of 4320 columns) and shall be supported for interoperability.

Figure 10.3 shows the TFI-5 3.1104 Gbps frame format (N = 60). This frame has the same dimensions as a SONET STS-60 or SDH STM-20 frame (9 rows of 5400 columns). Support of the TFI-5 3.1104 Gbps rate and frame format is optional.

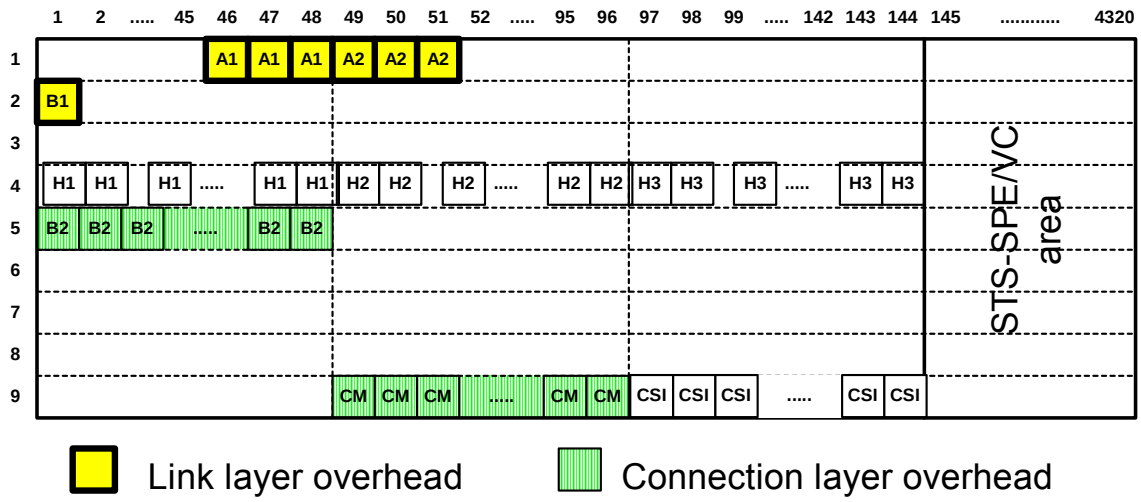


Figure 10.2 TFI-5 2.488 Gbps (STS-48) Frame Format (required support)

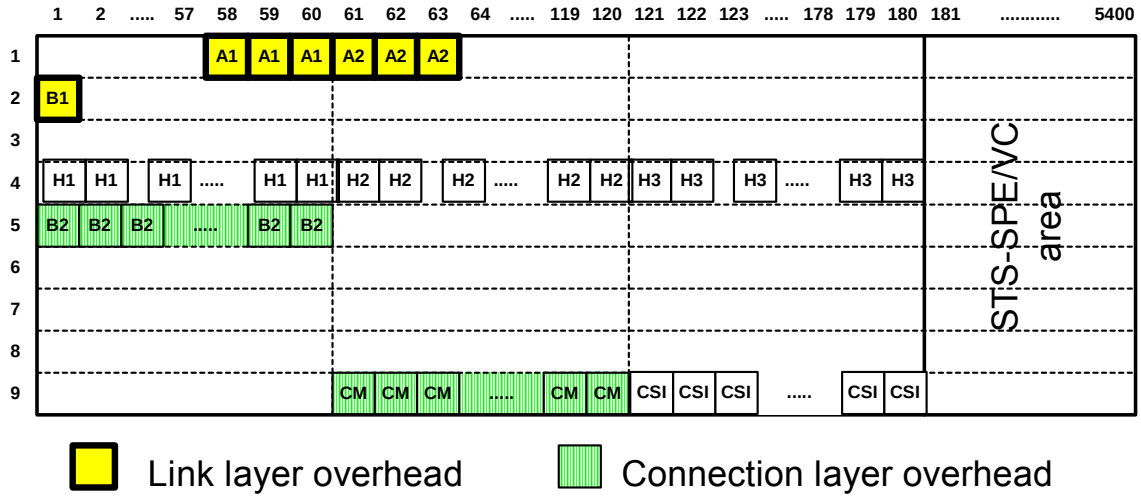


Figure 10.3 TFI-5 3.1104 Gbps (STS-60) Frame Format (optional support)

There are three layers defined for TFI-5: Link, Connection and Mapping. Figure 10.4 shows the hierarchical relation between the layers.

- The TFI-5 Link layer defines the operations performed and the information generated/terminated by the TFIDATA link source and sink devices. The TFI-5 Link layer is generated and terminated at each TFI-5 link.

- The TFI-5 Connection layer enables monitoring of the end-to end connection of each STS-1 time-slot from Ingress framer to Egress framer, passing through the TDM switch fabric.

- The TFI-5 Mapping layer performs the association and mapping of client signals to one or more STS-1 time-slots of the Connection layer. In order to carry client signals with bandwidths greater than that of a single TFI-5 link, the TFI-5 Mapping Layer can group a set of STS-1 time-slots transported in different TFI-5 links (inverse multiplexing).

Figure 10.5 shows the extent of each TFI-5 layer using a simplified STS-1 cross-connect model. This simplified model separates the Ingress framers (receivers) and the Egress framers (transmitters) in order to simplify the description.

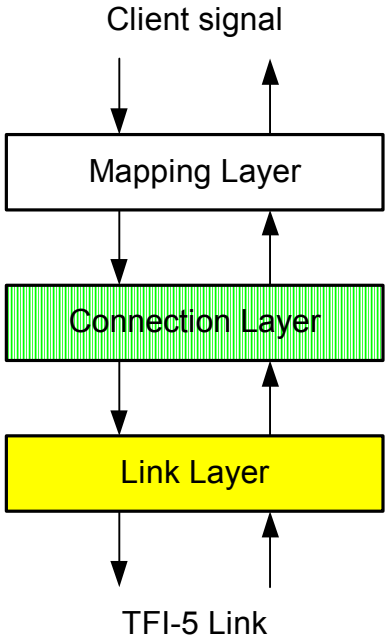


Figure 10.4 TFI-5 Layers

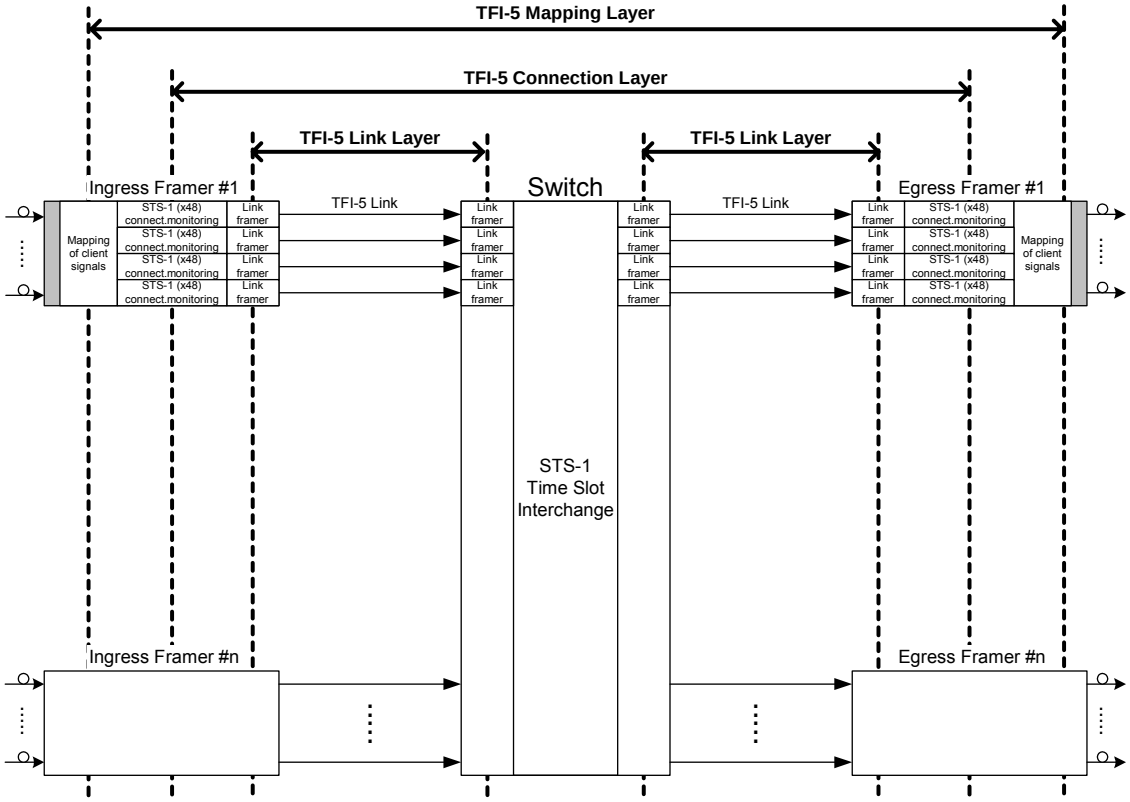


Figure 10.5 TFI-5 Layers Example (an STS-1 cross-connect)

10.1 TFI-5 Link Layer

The Link layer is generated and terminated at each TFI-5 link. The Link layer is independent of the client payload that forms the data stream multiplexed across a group of TFI-5 links. The Link layer embodies the electrical signaling and link rate specifications, link framing, link scrambling, link error monitoring and frame deskew functions. The Link layer operates on each link independently.

The Period of transmission of a TFI-5 frame is 125 µs. Two different baud rates are defined: the standard SONET/SDH 2.488 Gbps transmission rate and an optional 3.1104 Gbps transmission rate. Support of the 3.1104 Gbps transmission rate is not required.

The TFI-5 2.488 Gbps frame format is shown in Figure 10.2. The TFI-5 frame format for the optional rate 3.1104 Gbps is shown in Figure 10.3. The bytes and bits are transmitted as defined in [14, 15, 24]: the order of transmission of the TFI-5 frame bytes (Figures 10.2 and 10.3) is first from left to right and then from top to bottom. Within each byte the most significant bit is transmitted first.

The overhead bytes A1, A2 and B1 as shown in figure 10.1, 10.2 and 10.3 are used by the Link layer for frame delineation and supervision purposes. These bytes are generated by each TFI-5 link transmitter (TFI-5 link source device) and terminated by each TFI-5 link receiver (TFI-5 link sink device).

10.1.1 TFI-5 Frame Delineation (A1A2 bytes)

The TFI-5 frame shall contain three A1/A2 pairs (three A1 bytes followed by three A2 bytes) located in the first row. The three A1 bytes are located in columns N-2, N-1 and N, and the three A2 bytes are located in columns N+1, N+2 and N+3 (N = 48, 60). The source device of a TFI-5 link shall insert this 6-byte sequence. The A1 bytes carry the value 0xF6 and the A2 bytes carry the value 0x28.

The sink device of the TFI-5 link locates the TFI-5 frame boundaries by searching for the framing pattern contained In the A1 and A2 bytes as defined above. Implementations of TFI-5 framers may frame on a subset of the 3 A1 and 3 A2 bytes.

Upon startup or reset the sink device goes to the OOF (Out Of Frame) state (Figure 10.5.1). The sink device shall transition from the OOF state to the INF (In-Frame) state after finding the framing pattern, one TFI-5 frame apart (125 µs), for M_1 consecutive frame times. M_1 is defined to be 2 frames in this standard. Once in the INF state, the sink device shall continue to monitor for correct alignment. The sink device of the TFI-5 link shall transition from the INF state to the OOF state if the framing pattern is not found (at least one

incorrect bit) during M_2 consecutive frames. M_2 is defined to be less than or equal to 5 frames in this standard.

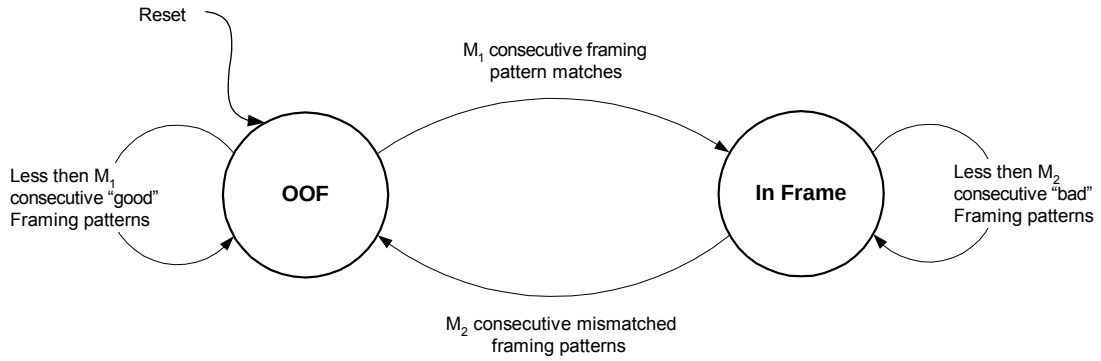


Figure 10.5.1 TFI-5 State Diagram for Out of Frame and In Frame Conditions

When the sink device of a TFI-5 link is in the OOF state it shall alert the downstream element by overwriting to "all ones" all of the bytes in the Connection and Mapping Layers.

10.1.2 TFI-5 Frame Scrambling

TFI-5 links are scrambled to ensure rich transition density. The TFI-5 link is scrambled with the SONET/SDH polynomial of $X^7 + X^6 + 1$. The scrambling is done in the same way as for a standard SONET/SDH frame, as per [14, 15, 24]:

- The residue of the scrambler is initialized to all ones on the most-significant bit of the byte in row 1 and column [3*N]+1 (N = 48, 60) of the TFI-5 frame: this is the first SPE byte of a SONET/SDH frame
- The scrambler is disabled for the bytes located in columns 1 to 3*N (N = 48, 60) of the first row: this is the whole first SOH row of a SONET/SDH frame.

As an option, it is possible to enable the scrambling of the bytes in columns 1 to N-3 and N+4 to 3*N (N = 48, 60) of the first row. The bytes in columns N-2 to N+3 (N = 48, 60) are never scrambled, but the scrambler shall continue to run during these byte positions. When this option is enabled, columns 1 to N-3 and N+4 to 3*N (N = 48, 60) of the first row of the current TFI-5 frame are scrambled with the scrambler running from the reset in the previous TFI-5 frame. This optional "STS-768-like" scrambling mode can be used to assure an adequate number of transitions when the positions in columns 1 to N-3 and N+4 to 3*N of the first row of the TFI-5 frame are used by the Mapping layer.

When bytes 1 to N-3 and bytes N+4 to 3N are used by the Mapping layer, and the standard SONET/SDH mode of scrambling is enabled, the content of these bytes must be compliant with ITU-T G.957 Appendix II: Consecutive Identical Digits (CID).

Scrambling by all devices in a TFI-5 system should utilize the standard SONET scrambling unless all devices on the link support the optional scrambling mode. For applications that use bytes 1 to N-3 and bytes N+4 to 3N as Mapping layer bytes where sufficient transition density cannot be ensured, it is a requirement to support the STS-768-like scrambling mode.

10.1.3 TFI-5 Link Error Monitoring (B1 byte)

TFI-5 links can be monitored using bit-interleaved (BIP-8) parity for transmission errors. The definition of the B1 byte is lifted directly from [14, 15, 24]. The B1 byte is located in the first column of the second row of the TFI-5 frame (see Figure 10.1) and carries a BIP-8 code using even parity. The BIP-8 is calculated over all the bytes in the previous TFI-5 frame after scrambling and is placed in the B1 byte of the current frame before scrambling.

In order to allow fault isolation the BIP-8 shall be calculated and inserted in the B1 byte by the source device of every TFI-5 link. The sink device of every TFI-5 link shall monitor the B1 byte.

10.1.4 TFI-5 Link Deskew

All TFI-5 links in a system have a 2.488 Gbps standard rate (or optionally a 3.1104 Gbps rate) and are frequency locked to a common clock reference (TFIREFCK). In order to be able to properly time-slot exchange different client payloads from multiple TFI-5 links across the fabric interfaces, the frame boundaries of the source links shall be closely aligned.

The start of a TFI-5 frame has a relative offset from the rising edge of TFI8KREF of (T) TFIREFCK cycles. T shall have a range of 1 full TFI8KREF cycle, and settable in increments of 8 TFIREFCK cycles or finer. The framer shall output the first A2 byte (byte N+1)of the frame at offset (T) with a timing accuracy of +/- 8 TFIREFCK cycles. Programmable offset (T) only applies to framers. The accuracy applies to both TFI-5 framers and switch fabrics.

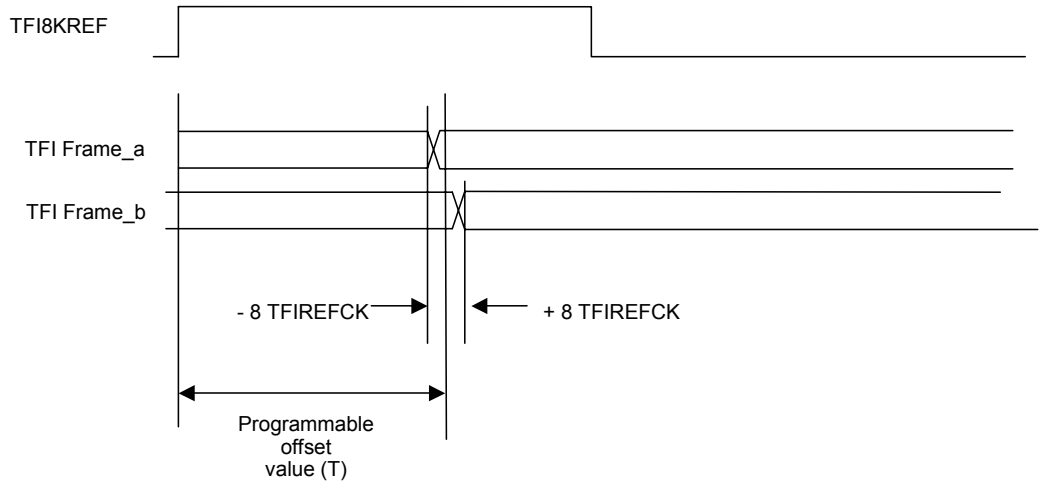


Figure 10.5.2 TFI-5 frame offset timing

When a set of TFI links contains client payloads that are to be switched or multiplexed together, the sink device receiving these links shall be able to tolerate total (skew + relative_wander/2) of at least 48 bytes. The arrival time between the earliest and latest arriving functional links at the sink device shall be less than 48 bytes.

Methods of achieving the standard TFI-5 alignment include pointer processing (retiming), multiplexing/inverse-multiplexing and mapping.

10.2 TFI-5 Connection Layer

The TFI-5 Connection layer is defined for each of the N STS-1 time-slots (N = 48, 60) transported inside a TFI-5 frame. The Connection layer extends end-to-end from the ingress framer to the egress framer. Optionally it provides for the following services for each STS-1 time-slot: supervision of errors and supervision of connectivity. The TFI-5 Connection layer uses the B2 and CM (Connection Monitoring) bytes as shown in Figures 10.1, 10.2 and 10.3 for these purposes.

10.2.1 TFI-5 Connection Error Monitoring (B2 byte)

Connection error monitoring is optional. The N B2 bytes (see Figure 10.1) are carried in columns 1 to N (N = 48, 60) of the fifth row of the TFI-5 frame (see Figure 10.1). These are the same positions as the B2 bytes in a standard SONET/SDH frame. One B2 byte is allocated in each STS-1 time-slot for a Connection layer bit-error monitoring function. Each B2 byte is a Bit

Interleaved Parity 8 code (BIP-8) using even parity. Each BIP-8 code is computed over all bits of the previous frame of the STS-1 time-slot (before Link layer scrambling) except the associated STS-1 time-slot bytes located in columns 1 to 3*N (N=48,60) of the first three rows of the TFI-5 frame. This BIP-8 code is placed in the B2 position of the current STS-1 time-slot. This is the same definition as for the standard SONET/SDH B2 bytes, where B2 is calculated over all bits of the Line OH and the Envelope Capacity of the previous STS-1 time-slot. If connection error monitoring is not used the B2 byte positions can be used by the TFI-5 Mapping layer. When connection error monitoring is implemented, a TFI-5 compliant device supporting this option shall provide means to disable B2 insertion at the source and B2 monitoring at the sink.

10.2.2 TFI-5 Connection Connectivity Monitoring (CM byte)

Connection connectivity monitoring is optional. The N CM bytes (see Figure 10.1) are carried in columns N+1 to 2*N of the ninth row of the TFI-5 frame (N = 48, 60). These are the same positions as the M0/M1/Z2 bytes in a standard SONET/SDH frame. The CM format is shown in Figure 10.6. The CM bytes allow the monitoring of each constituent STS-1 time-slot for switch misconnections.

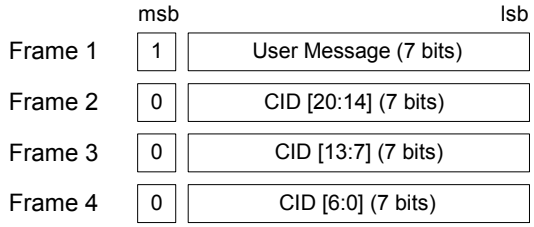


Figure 10.6 TFI-5 Connection Monitoring (CM) multi-frame format

The CM multi-frame spans four TFI-5 frames and carries a 7-bit User Message field and a 21-bit Connection Identifier (CID). Setting the most significant bit of the CM byte high shall identify the first frame in the CM multi-frame. The most significant bit of the CM bytes of the 3 remaining frames shall be set low.

When CM is implemented, the CID field shall be configurable by system software at the TFI-5 source device and shall be readable by system software at the sink device to uniquely identify every constituent STS-1 time-slot within every TFI-5 link within a system.

When CM is implemented, the TFI-5 sink process shall be able to monitor the CID field by comparing its value to the value of the expected CID in order to detect misconnections at the switch fabric. Persistence shall be used to prevent bit errors from causing connection management mismatches.

If connection connectivity monitoring is not used the CM byte positions can be used by the TFI-5 Mapping layer. When connection connectivity monitoring is implemented, a TFI-5 compliant device supporting this option shall provide means to disable CM insertion at the source and CM monitoring at the sink.

10.2.3 TFI-5 Connection forward defect indication

In case of a TFI-5 link failure (Loss of signal, out of frame) the down stream signal (connection and mapping layer) is set to “all ones”. This condition can be detected by a “1111 1111” code in the CSI bytes if CSI is supported. The generation of client signal specific forward defect indications (e.g. SONET/SDH AIS, ODU-FDI) has to be done in the egress framer and is outside the scope of the TFI-5 specification.

10.2.4 TFI-5 Connection open indication

If an STS-1 time-slot at the output of the TDM switch fabric is not connected to any input STS-1 time-slot all Connection and Mapping layer bytes of this time-slot shall be set to zero. This condition can be detected by a “0000 0000” code in the CM bytes if CM is supported. The generation of the client signal specific unequipped or open connection signal (e.g. STS-SPE/VC Unequipped, ODU Open Connection Indication) has to be done on the egress framer and is outside the scope of the TFI-5 specification.

10.3 TFI-5 Mapping Layer

The TFI-5 Mapping layer provides the transport of the client signals over one or more TFI-5 Connection layer time-slots. All the bytes of the TFI-5 frame that are not used by the Link and Connection layer are available for the Mapping layer (see Table 10.1).

If bytes of the TFI-5 frame are not used by the Mapping, Connection or Link layer they shall be undefined except for the bytes 1 to N-3 in row 1 which shall be set to 0xF6 and the byte N+4 to 2*N in row 1 which shall be set to 0x28.

The basic mapping scheme uses the SONET/SDH structure as defined in [14,15,24].

Non-SONET/SDH client signals can be transported across the TFI-5 by mapping them inside a concatenated group of SONET/SDH STS-3c SPEs/VC-4s. As all the TFI-5 signals are frame aligned and the payload frames are also aligned to a fixed pointer offset, no specific overhead for alignment is required within TFI-5 for transporting non-SONET/SDH clients.

Type	Name	Positions
Bytes that belong to the Link Layer	A1	Columns N-2 to N of the 1st row
	A2	Columns N+1 to N+3 of the 1st row
	B1	Column 1 of the 2nd row
Bytes that are optionally used by the Connection layer otherwise they may be used by the Mapping Layer	B2	Columns 1 to N of the 5th row
	CM	Columns N+1 to 2*N of the 9th row
Bytes that are optionally used for Client Status Indication otherwise they may be used for other Mapping Layer functions	CSI	Columns 2N+1 to 3*N of the 9th row
Bytes that are optionally used by the Mapping layer otherwise they default to 0xF6, 0x28, respectively	-	Columns 1 to N-3 of the 1st row
	-	Columns N=4 to 2*N of the 1st row
Bytes that belong to the Mapping layer for payload transport	All other	

Table 10.1 Layer Assignments of TFI-5 bytes

TFI-5 Client Status Indication (CSI byte)

Client Status Indication is optional. The Client Status Indication (CSI) bytes provide a mechanism for the framer to report the status of client signals and/or to send commands to the switch fabric. This information can be used to control protection switching on the switch fabric. The encoding of CSI is unique for each client type as the alarms and conditions are dissimilar.

Client Status Indication (CSI) is provided in a single byte (E2 byte in SONET/SDH) for each STS-1. The CSI bytes (see Figure 10.1) are carried in columns 2*N+1 to 3*N of the ninth row of the TFI-5 frame (N = 48, 60). The CSI byte shall be provisioned to the E2 SONET/SDH Transport Overhead (TOH) byte. Tables 10.2 and 10.3 show the relevant byte assignments:

The following rules apply to the generation and interpretation of CSI when it is implemented:

1. CSI codes are assigned in order of alarm/condition priority. (High priority alarm/conditions have high CSI code values).

2. The framer sets the CSI codes in all time-slots associated with each client to the same value

10.3.1 Mapping of SONET/SDH client signals

As a default SONET/SDH STS-1-SPE, STS-3c-SPE, STS-Nc-SPE, VC-4, VC-4Xc and higher order VC-3 are mapped into TFI-5 time-slots. For certain applications the transport of SONET/SDH TOH/SOH over the TFI-5 system can be supported.

10.3.1.1 Mapping of SONET/SDH STS-SPEs/higher order VCs clients

SONET/SDH STS-SPEs/higher order VCs clients are transported in a TFI-5 signal in the same way as they are transported in a STS-N/STM-N signal (see [14,15, 24]). An STS/AU structure, as defined in [5], is aligned to the TFI-5 frame, is constructed with the STS-SPE/higher order VC and pointer. (In this section, the term “STS/AU structure” is equivalent to SDH AU structure.) If the client is not already aligned to the TFI-5 frame or differs from the TFI-5 bit rate, pointer justification is required.

Note: SONET does not define a structure that is the equivalent to the SDH AU structure. In SONET terms the AU structure consists of the STS envelope capacity and the related H1, H2 and H3 pointer bytes in the TOH.

The STS/AU structure is mapped into the H1, H2, H3 pointer bytes and STS-SPE/VC payload area of the TFI-5 frame (see Figure 10.1).

An STS-1/AU-3 is mapped into a single TFI-5 time-slot.

- An STS-3c/AU-4 is mapped into 3 TFI-5 time-slots.
- Contiguous concatenated STS-3*Nc/AU-4-Nc signals are mapped into 3*N time-slots of a TFI-5 frame.
- A STS/AU structure that exceeds the capacity of a single TFI-5 signal is mapped to time-slots in several TFI-5 signals (disinter leaving). Figure 10.7 shows an example of mapping a STS-768 client onto a set of 16 TFI-5 links. After alignment to the TFI-5 frame, client bytes are taken in sets of 16 and placed onto TFI-5 links. Namely, bytes 1-16 are placed on TFI-5 link #1, bytes 17-32 on TFI-5 link #2, and bytes 241-256 on TFI-5 link #16. Figure 10.8 shows an example of mapping an STS-192/STM-64 client into a set of 4 TFI-5 links. After alignment to the TFI-5 frame, client bytes are taken in sets of 16 and placed onto TFI-5 links. Namely, bytes 1-16 are placed on link #1, bytes 17-32 are placed on link #2, and bytes 49-64 are placed on link #4. See ITU-T G.707.

- A STS/AU structure can use time-slots in different TFI-5 signals even if the structure doesn't exceed the capacity of a TFI-5 signal.

TFI-5 requires neither special processing nor overhead to carry virtually concatenated clients.

- Virtual concatenated signals are treated as individual STS-SPE/VC signals.
- A TFI-5 system supports any standard mixture of non-concatenated, contiguous and virtually concatenated signals.
- The STS-SPE/VC transported in a TFI-5 signal can come from several OC-N/STM-N signals (e.g. 4 OC-12 interfaces are supported by a TFI-5).
- The time-slot assignment in the TFI-5 signal may follow the time-slot assignment in the OC-N/STM-N interface signal. This assignment is not followed, for example, for framers with time-slot interchange.

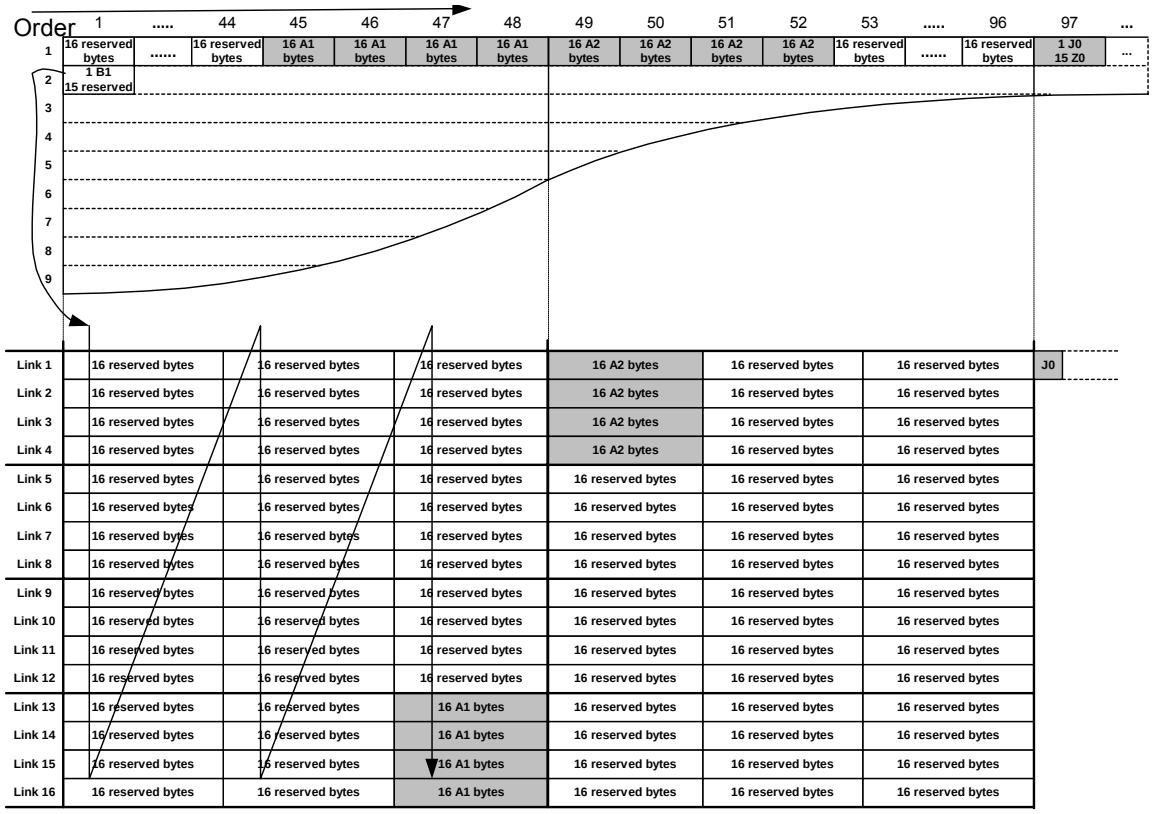


Figure 10.7 Example disinterleaving showing byte ordering of an STS-768 frame into 16 TFI-5 links

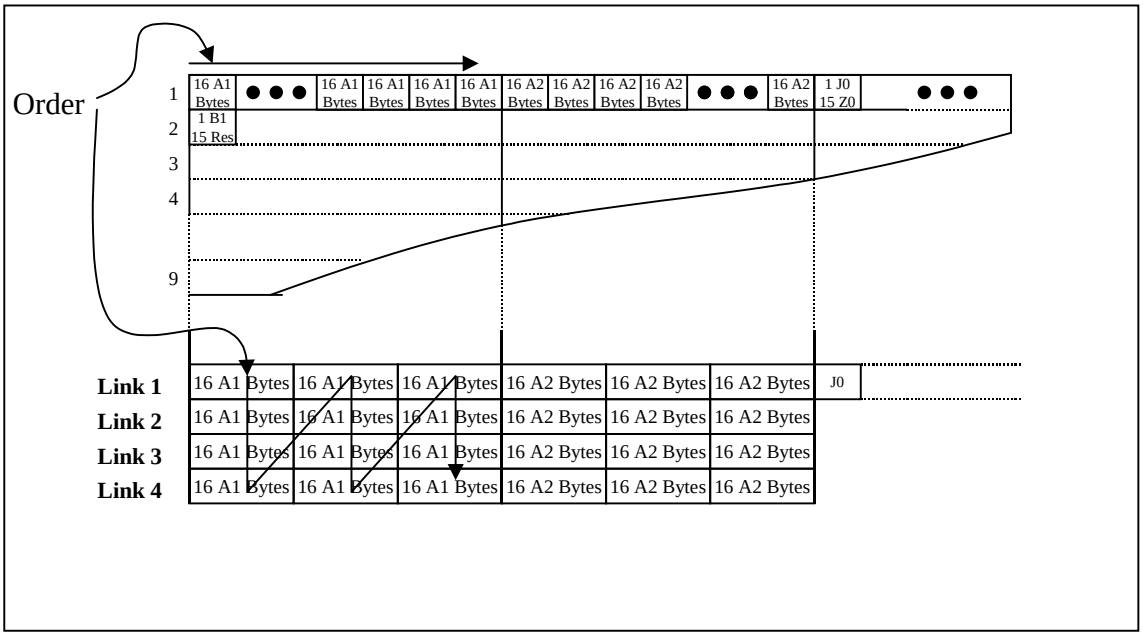


Figure 10.8 Example of disinterleaving showing byte ordering of an STS-192 frame into 4 TFI-5 links

10.3.1.2 TOH/SOH bytes

SONET section/line overhead (TOH), SDH regenerator/multiplex section overhead (SOH) and AU pointer bytes may be transported via a TFI-5 frame using the bytes 1 to 3*N in row 1 to 3 and 5 to 9 that are not used by the Link or Connection layers.

- The TOH/SOH bytes may be assigned to the same positions as in a standard SONET/SDH frame or use different positions (e.g. if the position is used by TFI-5). This is transparent to the TFI-5 signal and outside the scope of this implementation agreement.
- TOH/SOH bytes from a OC-N/STM-N signal may be distributed over several TFI-5 signals.
- A TFI-5 signal may transport TOH/SOH bytes from several OC-N/STM-N interfaces.
- Alignment of the TOH/SOH bytes to the TFI-5 clock is normally required. This alignment process is not standardized and outside the scope of the TFI-5 specification.

Note that the bytes in column 1 to 3*N belong to specific STS-1 time-slots of the TFI-5 Connection layer and take the same route as these time-slots in a TFI-5 system.

10.3.1.3 CSI coding for SONET/SDH clients

SONET/SDH status are encoded into the CSI byte as shown in Table 10.2 below.

CSI Code	Alarm/Condition
1111 1111	TFI-5 Link Loss of Signal
1111 1111	TFI-5 Link Loss of Frame
1111 1110	Software Force - Away
1111 1101	Software AIS Insert
1111 1100	Software Force-To
	Loss of Signal (LOS)
	Loss of Frame (LOF)
	Section Trace Identifier Mismatch (TIM-S)
	Line AIS (AIS-L)
	Signal Fail (SF-L) / Excessive BER (EXC-MS)
	Path AIS (AIS-P) / Concat AIS (AISC-P)
	Loss of Pointer (LOP) / Loss of Concat Ind (LOPC)
	Unequipped Signal Label (UNEQ)
	Path Trace Identifier Mismatch (TIM-P)
	Payload Label Mismatch (PLM)
	Signal Fail (SF-P) / Excessive BER (EXC-P)
	PDI-P code 28
	PDI-P code 27
	…
	PDI-P code 1
	Signal Degrade (SD-P)
	Signal Degrade (SD-L)
0000 0001	No Alarm
0000 0000	Reserved

Table 10.2 Client Status Indication (CSI) Coding for SONET/SDH clients

- The blank CSI code values are user programmable.

- Above each alarm/condition with a blank code point, there may be a user defined CSI alarm/condition entry. These may be used for augmenting the listed alarms/conditions with other simultaneously occurring alarms/conditions (e.g. Path alarm with SD-L).

- Generation of the CSI byte for alarms/conditions with blank code points are application dependent.

10.3.2 Mapping of OTN clients

The ODU1, ODU2 and ODU3 signals of the OTN (see [6]) are supported by a TFI-5 system. ITU-T defines the use of Virtual Concatenation for the transport of an OTN entity over SDH paths. Diverse routing of the VC-4-Xv's (X=17,68) requires large deskew buffers and H4 byte processing. Within the TFI-5 system, however, the differential delay between the different VC-4's (members of a group) is limited to 48 bytes. Therefore, the transport of an ODUk through a TFI-5 system does not require the implementation of any virtual concatenation mechanisms such as differential delay compensation and H4 processing as defined in [14,15, 24].Table 10.3 shows the C-4-Xc structure used for mapping and the number of STS-3c/VC-4's time-slots required for transport of the different ODUk signals within the TFI-5 system.

Client Signal	Nominal Bit Rate (Mb/Sec)	ITU-T Mapping	# STS-3c/VC-4's time-slots required for transport within TFI-5 system
ODU1	2498.775126	C-4-17c	17
ODU2	10037.273924	C-4-68c	68
ODU3	40319.218983	C-4-272c	272

Table 10.3 Transport of OTN entities over TFI-5 link(s) via STS-3c/VC-4 Time-slots

10.3.2.1 Mapping of a ODU1 client signal

The transport of a ODU1 client signal across a TFI-5 shall be done by mapping the ODU1 into a C-4-17c as defined in [7] and by transporting this concatenated container over 17 STS-3c-SPE/VC-4. The active offset of the VC-4 shall be 522 (pointer offset value) for ODU1 mappings.

Figure 10.4.2 details how the C-4-17c structure carrying an ODU1 after being mapped is transported through a TFI-5 system using 17 STS-3c/VC-4 time-slots: the C-4-17c concatenated structure is column disinterleaved over the 17 STS-3c/VC-4 time-slots. The 17 VC-4's generated in this way are aligned to the pointer value of 522 and then transported over any combination of TFI-5 links. The first column of the STS-3c/VC-4 time-slots (equivalent bytes J1, B3, C2, etc… in a SONET/SDH frame) are unused (see Figure 10.4.2) and have undefined value. The STS-3c/VC-4 time-slots can be striped over multiple TFI-5 links, or multiplexed and carried over 1 or more links. See Section 10.2.2 for information on the Connectivity Monitoring (CM byte).

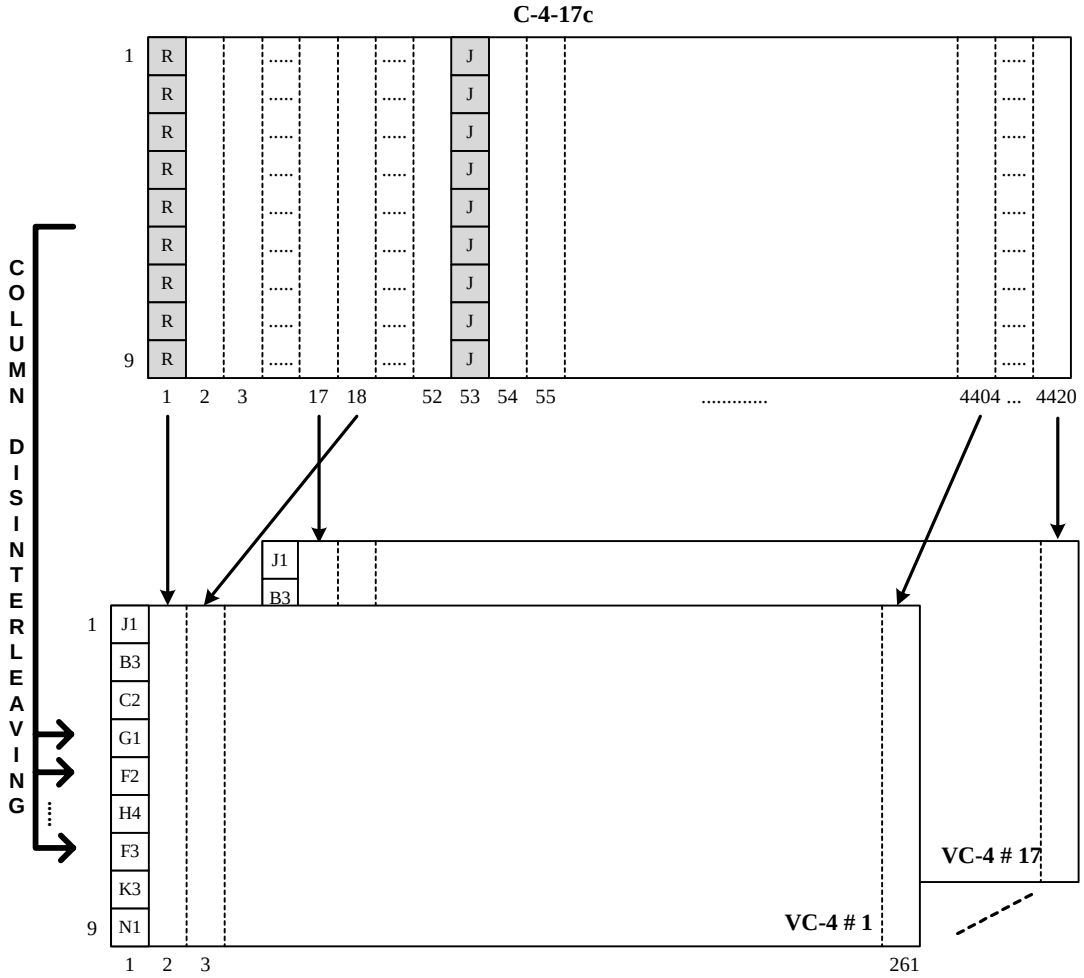


Figure 10.4.2: Disinterleaving of a C-4-17c for transport over TFI-5 link(s) using 17 STS-3c/VC-4 time-slots

Figure 10.4.3 details the reconstruction of the C-4-17c from the 17 STS-3c/VC-4 time-slots (received from any combination of TFI-5 links). The 17 STS-3c/VC-4 time-slots, are column interleaved to obtain the C-4-17c.

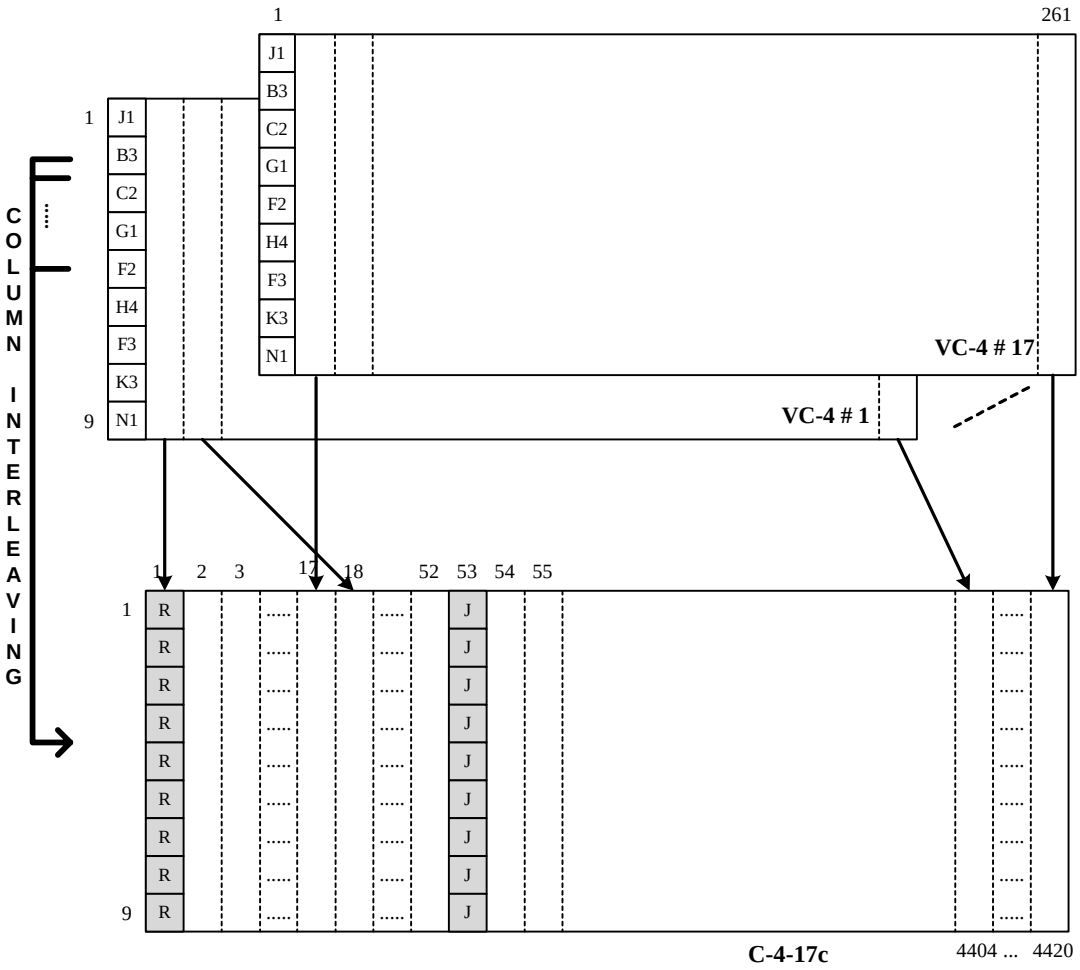


Figure 10.4.4: Interleaving of a C-4-17c from 17 STS-3c/VC-4 time-slots

10.3.2.2 Mapping of a ODU2 client signal

The transport of a ODU2 client signal across a TFI-5 shall be done by mapping the ODU2 into a C-4-68c as defined in [7] and by transporting this concatenated container over 68 STS-3c-SPE/VC-4. The active offset of the VC-4 shall be 522 (pointer offset value) for ODU2 mappings.

Figure 10.4.5 details how the C-4-68c structure carrying an ODU2 after being mapped is transported through a TFI-5 system using 68 STS-3c/VC-4 time-slots: the C-4-68c concatenated structure is column disinterleaved over the 68 STS-3c/VC-4 time-slots. The 68 STS-3c/VC-4's generated in this way are aligned to the pointer value of 522 and then transported over any combination of TFI-5 links. Columns 3N+N (N=48,60) of the TFI-5 frame (Equivalent bytes J1, B3, C2, etc… in a SONET/SDH frame) are unused (see Figure 10.1) and have undefined value. The STS-3c/VC-4 time-slots can be striped over multiple TFI-5 links, or multiplexed and carried over 4 or more links. For OTN client mappings, the POH overhead bytes are undefined. See Section 10.2.2 for information on the Connectivity Monitoring (CM byte).

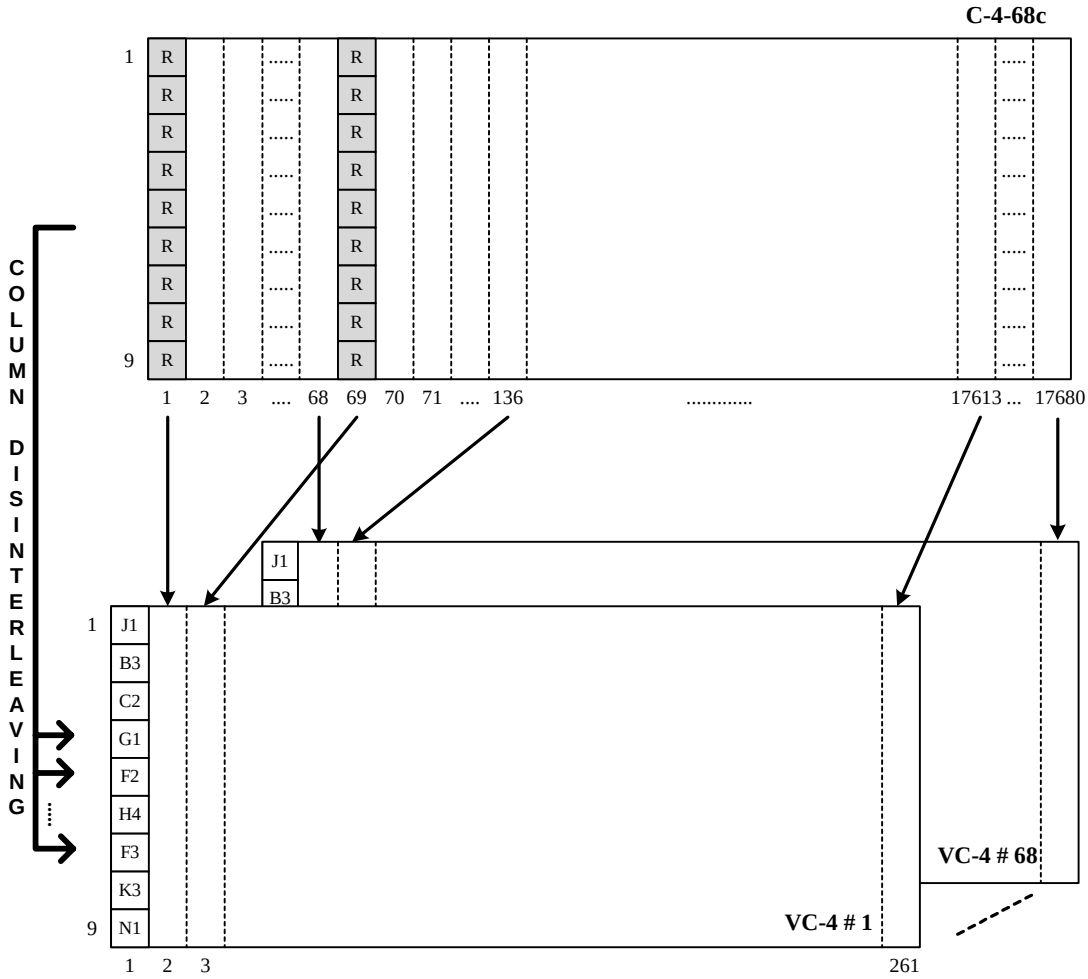


Figure 10.4.5: Disinterleaving of a C-4-68c for transport over TFI-5 link(s) using 64 STS-3c/VC-4 time-slots

Figure 10.4.6 details the reconstruction of the C-4-68c from the 68 STS-3c/VC-4 time-slots (received from any combination of TFI-5 links). The 68 STS-3c/VC-4 time-slots, are column interleaved to obtain the C-4-68c.

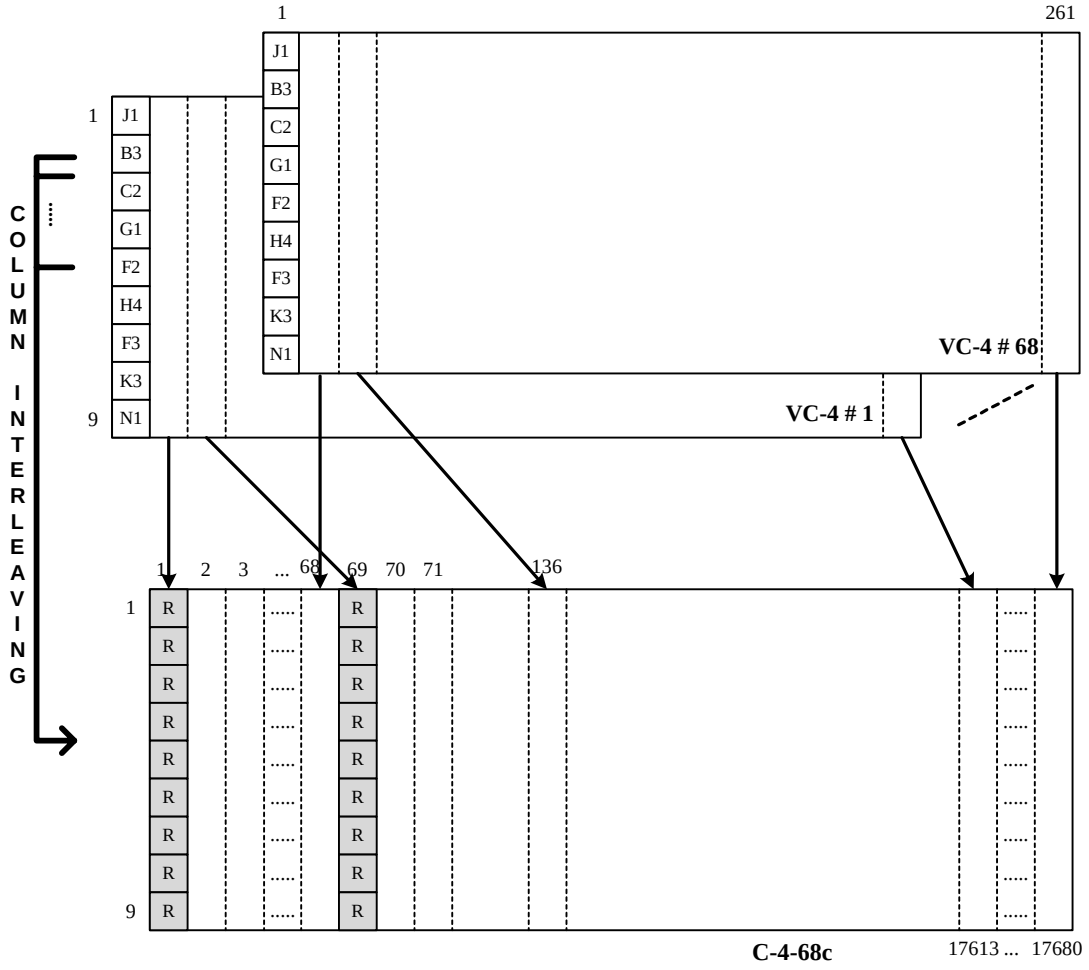


Figure 10.4.6: Interleaving of a C-4-68c from 68 STS-3c/VC-4 time-slots

10.3.2.3 Mapping of a ODU3 client signal

The transport of a ODU3 client signal across a TFI-5 shall be done by mapping the ODU3 into a C-4-Xc (a possible mapping is given in Appendix A.1) and by transporting this concatenated container over n STS-3c-SPE/VC-4. The active offset of the VC-4 shall be 522 (pointer offset value) for ODU3 mappings.

10.3.2.4 CSI Coding for OTN clients

OTN status is encoded into the CSI byte as shown in Table 10.4 below.

CSI Code	Alarm/Condition
1111 1111	TFI-5 Link Loss of Signal
1111 1111	TFI-5 Link Loss of Frame
1111 1110	Software Force - Away
1111 1101	Software AIS Insert
1111 1100	Software Force-To
	Loss of Signal (LOS)
	OTUk AIS (AIS-OTUk)
	Loss of Frame (LOF)
	Loss of Multi-Frame (LOM)
	OTUk Trail Trace Identifier Mismatch (TIM-OTUk)
	OTUk Signal Fail / Excessive BER (SF-OTUk)
	ODU Open Connection Indication (OCI-ODUk)
	ODUk Locked Defect (LCK-ODUk)
	ODUk AIS (AIS-ODUk)
	ODUk Trail Trace Identifier Mismatch (TIM-ODUk)
	ODUk Signal Fail / Excessive BER (SF-ODUk)
	ODUk Signal Degrade (SD-ODUk)
	OTUk Signal Degrade (SD-ODUk)
0000 0001	No Alarm
0000 0000	Reserved

Table 10.4: Client Status Indication (CSI) Coding for OTN clients.

- The blank CSI code values are user programmable.

- Above each alarm/condition with a blank code point, there may be a user defined CSI alarm/condition entry. These may be used for augmenting the listed alarms/conditions with other simultaneously occurring alarms/conditions

- Generation of the CSI byte for alarms/conditions with blank code points are application dependent.

10.3.3 Mapping of Ethernet clients

10 GE signals as defined in [8] are supported by a TFI-5 system.

10.3.3.1 Mapping of 10 GbE LAN PHY

The transport of a 10 GbE LAN PHY client signal across a TFI-5 shall be done by mapping the 10 GbE LAN PHY into a C-4-Xc (a possible mapping is given in Appendix A.2) and by transporting this concatenated container over n STS-3c-SPE/VC-4. The active offset of the VC-4 shall be 522 (pointer offset value) for 10GE LAN PHY mappings. For 10 GbE LAN PHY mappings, the POH overhead bytes are undefined.

10.3.3.2 Mapping of 10 GbE WAN PHY

The 10 GbE WAN PHY is based on a OC-192/STM-64 signal with a STS-192c-SPE/VC-4-64c. It is treated like standard SONET/SDH signals in a TFI-5 system.

11. Electrical Interface Definition

This section describes the signaling that allows for TFI-5 link operation at 2.488 Gbps to 3.11 Gbps. The specification defines the characteristics required to communicate between an TFI-5 driver and an TFI-5 receiver using copper signal traces across a communication backplane consisting of approximately 30 inches (76 cm) of total PCB trace including two connectors. The characteristic impedance of the signal traces is nominally 100 ohms differential. Connections are point-to-point and signaling is unidirectional. TFI-5 devices from different manufacturers shall be inter-operable.

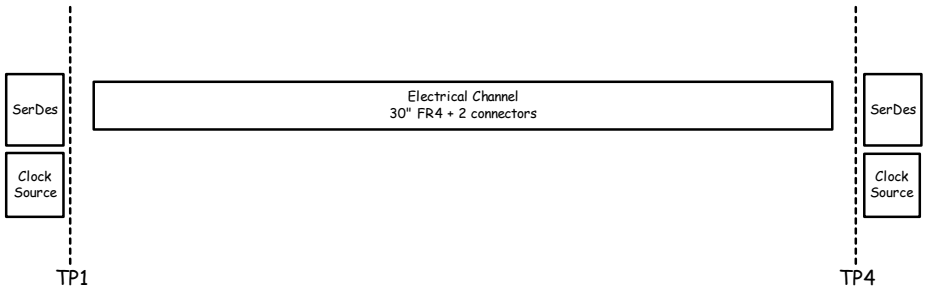
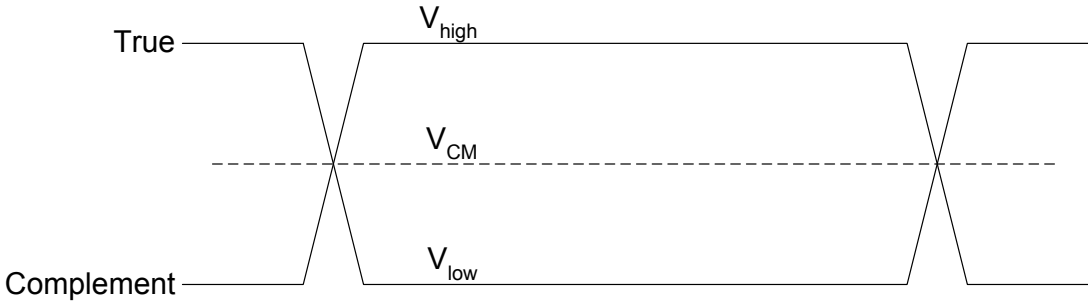


Figure 11.1 TFI-5 application model for the pure electrical interface, also called the intra-rack system.

Differential signaling conventions are shown in Figure 11.2 below. The differential amplitude represents the value of the voltage between the true and complement signals. Peak-Peak voltage is defined as $2*(V_{high} – V_{low})$. The common mode voltage is the average of V_{high} and V_{low}.

Figure 11.2 General Signal Definition



11.1 Differential Output Characteristics

Output parameters that can be derived from other specified parameters may not be explicitly specified. The use of external DC blocking capacitors is optional. Any loss or jitter caused by these capacitors must be accounted for as part of the allocation for the printed circuit board on which the capacitors reside.

The frequency dependent attenuation of the inter-connection media degrades the signal and thus produces inter-symbol interference or data dependent jitter. Given this and the receiver eye mask, transmit emphasis shall be required.

All TFI-5 output drivers shall meet all the parameters of Table 11.1. The receiver eye mask is provided in Figure 11.6 and Table 11.3 and assumes the TFI-5 channel model (See the Channel Model Section below). This allows maximum design flexibility while still guaranteeing interoperability. Transmitter interoperability shall be tested using the methodology described in the OIF CEI IA section 2.2.3

Symbol	Parameter	Max	Min	Units	Comments
Vod	Output Differential Voltage	1.4		Vppd	Min is implied given channel and receiver eye mask
Voh	Output High Voltage	2.3		V	AC coupled. If DC coupled parameter can be calculated from Vod and Vcm.
Vol	Output Low Voltage		-0.1	V	AC coupled. If DC coupled parameter can be calculated given Vod and Vcm.
V_{CM}	Output Common Mode Voltage	Vtt	0.62	V	$(V_{high} + V_{low}) / 2$. When using a load of Figure 11.3 with $1.05V<V_{tt}<1.35$, $75< R_D <125$ ohms, $0<Zvtt<30$ ohms. Ground in Figure 11.3 is to be the same potential as the driver ground. (see note 1) Parameter is unspecified if DC blocking capacitors are present.
T_{DRF}	Driver Rise/Fall Time		50	ps	At 20% - 80% into 100 ohm load
I_{DSHORT}	Short Circuit Current	70	-70	mA	Resulting DC current from a forced voltage when the Tx is powered on or off. See note 2 and Figure 11.5.
UI_D	Unit Interval	402	321	ps	2.488 Gbps to 3.11 Gbps, ±100 ppm
R_{SE}	Single-ended output impedance	62.5	37.5	Ohm	at DC
R_D	Differential Impedance	125	75	Ohm	at DC
RL_{SE}	Single-ended return loss		7.5	dB	From 0.004*baud rate to 0.75*baud rate
RL_{OUT}	Differential return loss		7.5	dB	From 0.004*baud rate to 0.75*baud rate

Table 11.1: TFI-5 Output Characteristics

Notes

1. *The Vtt values take into account a maximum of +/-50mv ground shift between transmit and receiver. If higher values in ground shift are within the system, then AC coupling should be used.*
2. *Current after 10μS to any voltage between –0.05 and 1.45V if DC coupling allowed or required, or between –0.05 and 2.35V if AC coupling allowed or required. The time 0μS is defined as the instant when the applied voltage is turned on. dV/dT changes within this range are to be below 1V/μS. See Figure 11.5 for more info.*

11.2 Differential Input Characteristics

All TFI-5 input receivers shall meet all the parameters of Table 11.2, Figure 11.3 and Figure 11.5. Also the receive eye mask of Table 11.3 and Figure 11.6 must be met.

Symbol	Parameter	Max	Min	Units	Comments
V_{tt}	Termination Voltage	1.30	1.10	V	Parameter unspecified if DC blocking capacitors are present
Z_{Vtt}	Bias Voltage Source Impedance	30		Ohm	From DC to .75*baud rate if DC blocking capacitors are not present. From 500Mhz to .75*baud rate if DC blocking capacitors are present. (see note 1)
V_{RCM}	Input Common Mode Voltage	Vtt	0.6	V	$(V_{high} + V_{low}) / 2$, (see note 2) Parameter unspecified if DC blocking capacitors are present
Z_{INDIFF}	Differential input impedance	125	75	Ohm	At DC as in Figure 11.3. If AC coupled, parameter applies at 0.0035*Fd only
RL_{IN}	Differential return loss		10	dB	From 0.004*baud rate to 0.75*baud rate relative to 100 ohms
Ioff	Current when powered off	50	-50	mA	Resulting DC current from a forced voltage. See note 3
Vrpp	Voltage without damage	1.45	-0.25	V	See note 4

Table 11.2: TFI-5 Differential Input Characteristics

Notes

1. *Magnitude of complex impedance with real part >0*
2. *Maximum of up to +/-50mv ground shift between transmit and receiver. If higher values in ground shift are within the system, then AC coupling should be used.*
3. *Current after 10μS to any voltage between –0.05 and 1.45V if DC coupling allowed or required, or between –0.05 and 2.35V if AC coupling allowed or required. The time 0μS is defined as the instant when the applied voltage is turned on. dV/dT changes within this range are to be below 1V/μS. See Figure 11.5 for more info.*
4. *Receiver shall not be damaged within the voltage range (powered on or off), dV/dT changes within this range are assumed to be below 1V/μS*
5. *For amplitude and rise/fall time requirements see the eye diagram of Figure 11.6.*

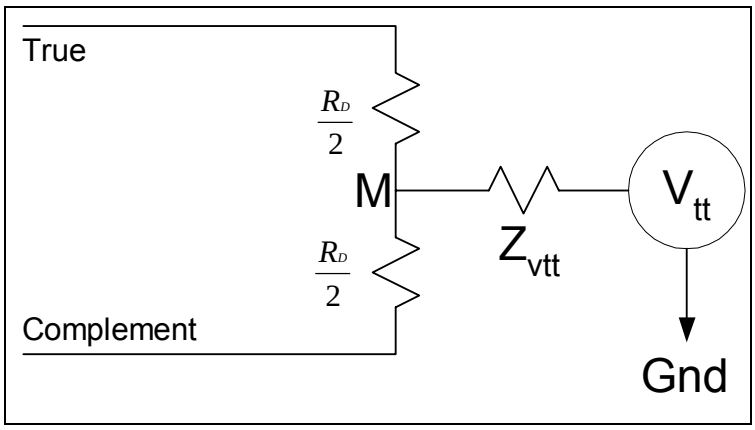
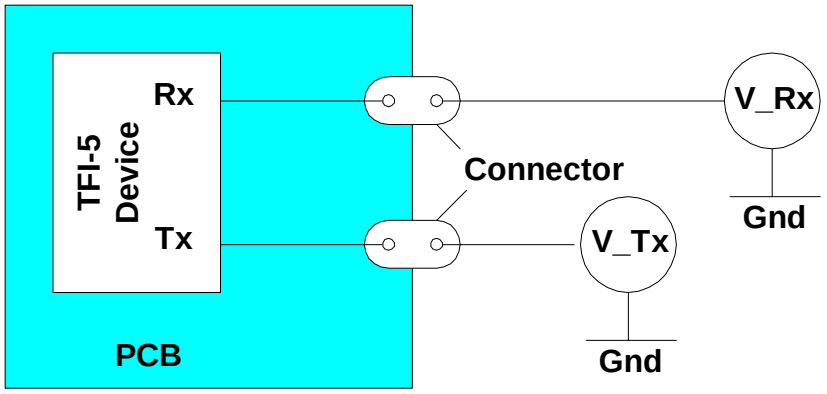


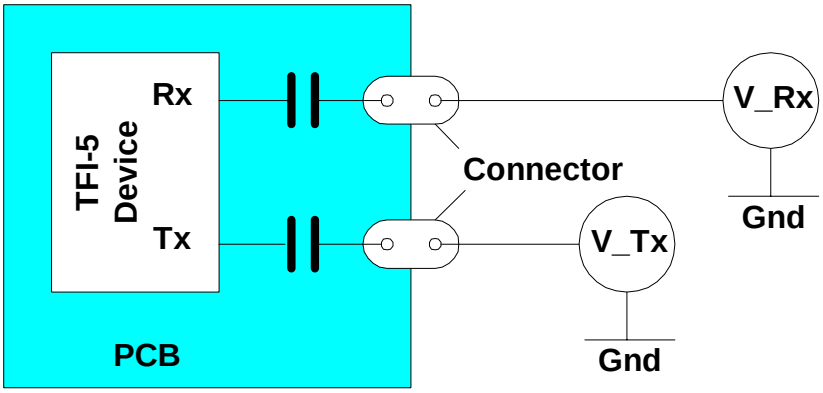
Figure 11.3 Termination and Signaling



$-0.05^{V} < V\_Rx < 1.45^{V}$
$dV/dT|_{max} = 1v/\mu S$
Resulting current after 10μS= +/-70mA

$-0.05^{V} < V\_Tx < 1.45^{V}$
$dV/dT|_{max} = 1v/\mu S$
Resulting current after 10μS= +/-70mA

a) Devices that are DC Coupled or can be DC coupled

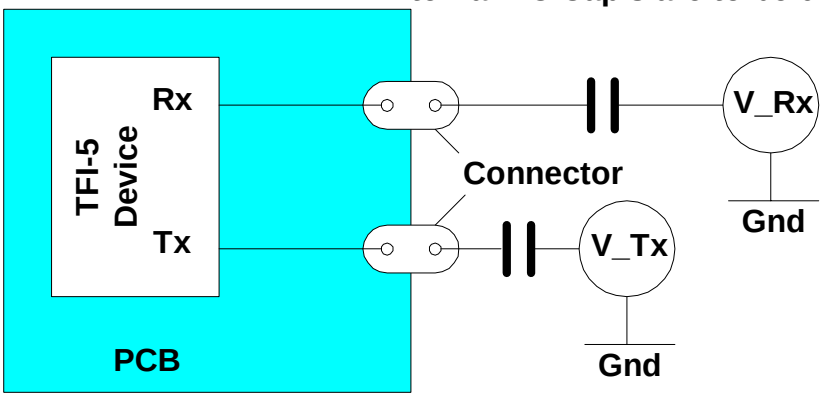


$-0.05^{V} < V\_Rx < 2.35^{V}$
$dV/dT|_{max} = 1v/\mu S$
Resulting current after 10μS= +/-70mA

$-0.05^{V} < V\_Tx < 2.35^{V}$
$dV/dT|_{max} = 1v/\mu S$
Resulting current after 10μS= +/-70mA

b) Devices that are AC Coupled on the PCB

External AC Cap's are to be 0.1μF



$-0.05^{V} < V\_Rx < 2.35^{V}$
$dV/dT|_{max} = 1v/\mu S$
Resulting current after 10μS= +/-70mA

$-0.05^{V} < V\_Tx < 2.35^{V}$
$dV/dT|_{max} = 1v/\mu S$
Resulting current after 10μS= +/-70mA

c) Devices that are AC Coupled on the other PCB or could be AC coupled

Figure 11.4 Idshort, Ioff & Vrpp Testing

11.3 Jitter Requirements

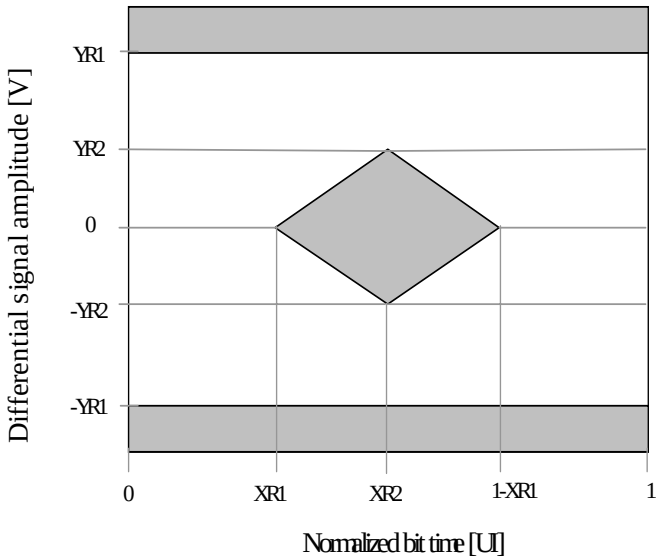
11.3.1 Compliant Channel

A channel with crosstalk is compliant if it is capable of meeting the receiver eye mask as specified in Figure 11.6 and Table 11.3 as per CEI IA section 2.2.2, with the following conditions:
1. A single post tap transmitter, with less than or equal to 6dB of emphasis in the post tap
2. No Rx equalization
3. A transmit amplitude of 350 mVppd
4. Additional non-ISI DJ jitter of 0.175UIpp (emulating part of the Tx jitter, not including any effects of post tap)
5. Additional non-ISI RJ jitter of 0.175UIpp (emulating part of the Tx jitter)
6. A Tx edge rate filter: simple 20dB/dec low pass at 75% of baud rate
7. At a baud rate of 3.11 Gbps
8. At a BER of 10-12

11.3.2 Receive Eye Mask

The receive eye mask specifies the jitter and amplitude at the receiver as shown in Figure 11.6. The horizontal limit specified in the eye mask shown in Table 11.3 represents the total jitter seen at the receiver input (both RJ and DJ). As per CEI IA section 2.2.4, the receiver shall tolerate at least the receiver eye template and jitter requirements as given in Table 11-3 with an additional sinusoidal jitter (Sj) as specified in section 11.4.

Figure 11.5 Receive Eye Mask



XR1 (UI)	XR2 (UI)	YR1 (V)	YR2 (V)	DJ [pp UI]	Total Jitter [pp UI]
0.33	0.5	0.7	0.0875	0.37	0.65

Table 11.3: Receive Eye Mask Specifications

Notes

1. *XR1, XR2, YR1 and YR2 are defined in Figure 11.6*
2. *XR1 = $J_{tot}/2$*
3. *Receive eye mask is measured into a 100 ohm load with more than 20 dB return loss between DC and 1.6 * baud rate.*
4. *Eye mask is the result of the jitter being passed through a single pole high pass filter with a corner frequency of baudRate/1667.*
5. *RJ is calculated as being the difference between total jitter and deterministic jitter.*
6. *The receiver eye mask is for a Bit Error Ratio (BER) of 10^{-12}*

11.4 Wander Requirements

The receiver shall be able to tolerate sinusoidal jitter as defined in Figure 11.8 that is summed with the receive jitter when the receive Dj term is reduced by 0.1 UI.

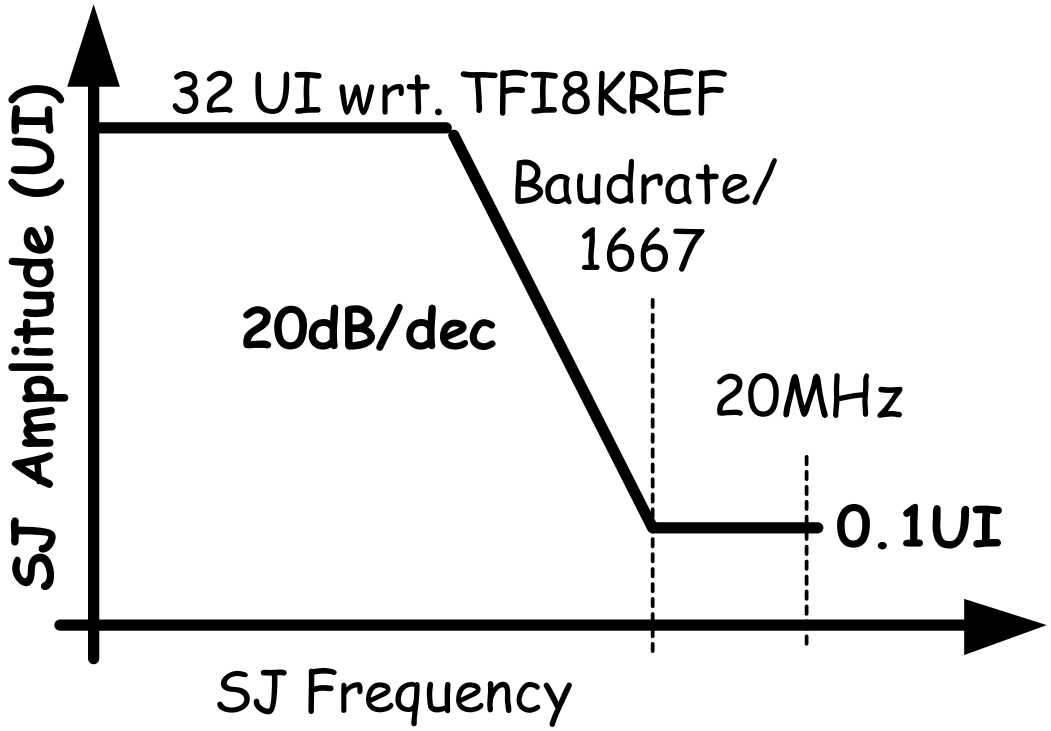


Figure 11.6 Sinusoidal Jitter allowable amplitude vs. frequency. Note that relative wander from one lane to another can be twice the absolute wander of 32 UI shown in this diagram.

12. Optical Interface Definition

This section describes the optical interface for TFI-5.

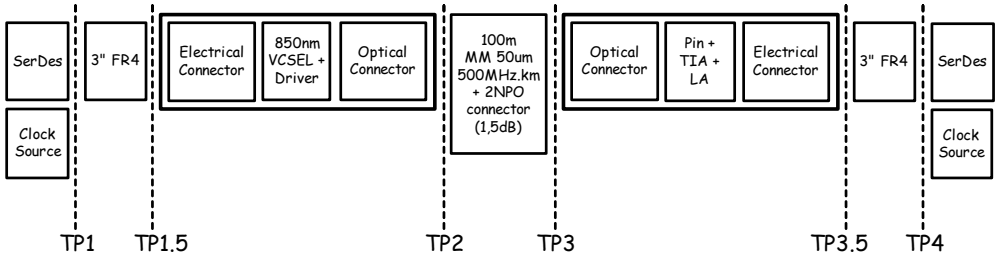


Figure 12.1: Electro-optical inter-rack application model

Notes:

1. Pre-emphasis may have to be considered at the output of the SerDes in order to achieve the jitter budget at TP2.
2. A possible hybrid inter-rack system with 30" FR4 as opposed to 3" FR4, would require a retimer after the 30" conforming to the electrical specification of the intra-rack system.

Figure 12.1 shows the application model of the TFI-5 optical link, referred to as the inter-rack application. The TFI-5 optical interface utilizes vertical-cavity surface-emitting lasers (VCSEL) and a fiber cable to transmit the TFI-5 frame over distances of up to 100 meters. The fiber solution leverages the parallel fiber VCSEL-based technology currently being deployed in many optical backplane applications for digital cross-connect systems, terabit routers and terabit switches. The target performance of the TFI-5 interface is to transmit data over 100 meters on standard 50-µm multimode fiber-ribbon cable.

Parameter	Min.	Max	Units
Transmitter[1]			
Transmitter P_{OUT} (avg)	-8[1]	-2.5[1]	dBm
Transmitter OMA	-7.2		dBm
λ_c	830	860	Nm
$\Delta\lambda_{rms}$		0.85	nm
T_{rise}/T_{fall} (20-80%)		130	ps
RIN(OMA)		-118	dB/Hz
Receiver[2,3]			
Receiver P_{IN} (avg)		-2.5	dBm
Receiver OMA[4]	-14		dBm
P_{STRESS} OMA [5]	-11.5		dBm
λ_c	830	860	nm
Return loss	12		dB
Signal detect – asserted[6]		-17	dBm
Signal detect – deasserted[6]	-30		dBm

Table 12.1 Optical Interface Specifications

Notes:
1. All specifications are per channel and at the end of a 2 m patch cord. In the event of accidental transmitter-to-transmitter connection, no damage shall occur that shall prevent the continued operation of the transmitter module within specification. Output power for combined channels shall be compliant with IEC Class 1M laser safety requirements of IEC 60825-1, Amendment 2 (all channels aggregated).
2. All receiver specifications are per channel.
3. Receiver sensitivity shall be such that the BER $\leq 10^{-12}$ with the minimum optical power and worst case extinction ratio.
4. Unstressed receiver sensitivity assuming no bandwidth penalties.
5. Assuming 2.5 dB penalty for jitter and clock and data recovery. Stressed receiver modulation and stressed compliance signal vertical eye closure values are calculated theoretically and are informative.
6. Average signal power at worst-case extinction ratio. Signal detect signal is asserted when all monitored channels are active. Signal is de-asserted when the optical power of one or more of the monitored channels drops below threshold.

12.1 Optical cable, cable plant specification and link budget

The optical fiber cabling model is shown in Figure 12.2.

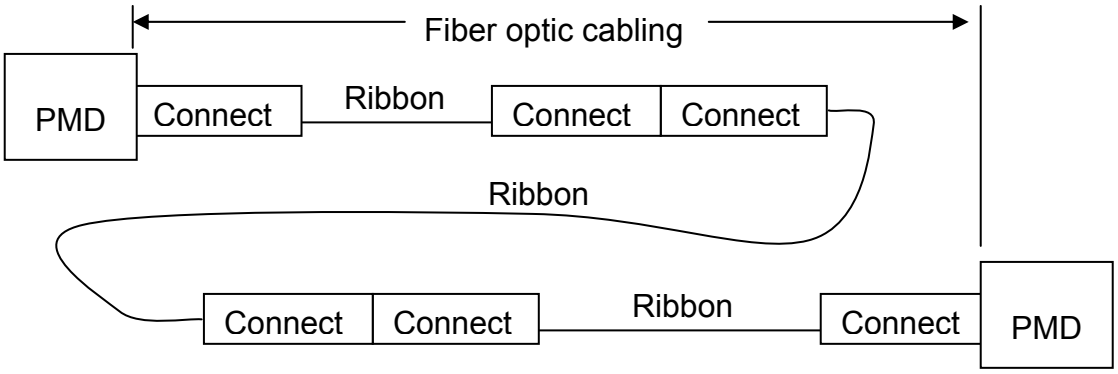


Figure 12.2 Fiber optic cabling model

. Each fiber shall carry a separate channel. The term channel is used for consistency with generic cabling standards.

Description	min	max	unit
Operating Wavelength	830	860	nm
Symbol rate per channel[7]		2.488	Gbaud
Modal Bandwidth[1]	500		MHz·km
Fiber attenuation at 850 nm		3.5	dB/km
Channel Insertion Loss (connectors + fiber loss) [3]		1.85	dB
Link Power Budget	6.8		dB
Jitter mask[5] parameter *W*, [Dj] at test point 2		0.26	UI
Jitter mask[5] parameter σ [Rj 1 σ] at test point 2		16	mUI
Jitter mask parameter W, [Dj] at test point 3		0.26	UI
Jitter mask parameter σ [Rj 1 σ] at test point 3		18	mUI
Operating range	2	100	m

Table 12.2 Multimode cable link power budget

1. Modal bandwidth at 830nm per TIA/EIA 455-204 or IEC 60793-1-40.
2. Link penalties are used for link budget calculations. These are not requirements and are not to be tested.
3. Jitter mask according to IEEE 802.3ae 10G-BASE-SR.
4. Test points are defined in the application model. In addition TP2 must be measured after a 2m patch cord. See Figure 12.1 for the location of test point TP2
5. Jitter budgets are given in Appendix B.

Appendix A: Mapping and Transport of ODU3 and 10gigE LAN PHY

The ODU3 and 10GE LAN mappings described here are simply proposals within the OIF and are potentially subject to standardization in other bodies. This material should be treated as informative only.

A.1 Asynchronous mapping of ODU3 into a C-4-272c for transport over 272 VC-4 / STS-3c's

The basic C-4-272c structure is comprised of 9 rows by 70720 (i.e. 272 x 260) columns. The extended ODU3 is mapped into this C-4-272c with the following structure (see Figure A.1):

1. Each of the nine rows is partitioned into 136 blocks, consisting of 520 octets each.

2. In each block, one negative justification opportunity octet (S) and five justification control bits (C) are provided.

3. Each block is partitioned into 5 sub-blocks, consisting of 104 octets each.

    a. The first byte of each sub-block consists of a justification control byte (J), which consists o seven fixed stuff bits (bits R; bits 1 to 7) and a justification control bit (bit C, bit 8).

    b. The second byte of the last sub-block is a negative justification opportunity byte (S).

    c. The last 103 bytes of the first four sub-blocks consist of data bytes (D).

    d. The last 102 bytes of the last sub-block consist of data bytes (D).

4. Before the extended ODUk signal is mapped into the C-4-Xc, it is scrambled using a self-synchronizing scrambler with polynomial X43 + 1. The scrambler operates over the whole ODUk frame and is not reset per frame. (See G.707 for details [5]).

The set of five justification control bits (C) in every block is used to control the corresponding negative justification opportunity byte (S). CCCCC = 00000 indicates that the S byte is an information byte, whereas CCCCC = 11111 indicates that the S byte is a justification byte.

At the synchronizer all five C bits are set to the same value. Majority vote (3 out of 5) should be used to make the justification decision at the desynchronizer for protection against single and double bit errors in the C bits.

The value contained in the S byte when used as justification byte is all-ZERO's. The receiver is required to ignore the value contained in this byte whenever it is used as a justification byte.

The value contained in the R bits and bytes is all-ZERO's. The receiver is required to ignore the value contained in these bits/bytes.

When ODU or 10 GbE LAN PHY are transported via TFI-5 pointer justification is not needed. Any frequency alignment between the ODU or 10 GbE LAN PHY clock and the TFI-5 clock is done via the byte stuffing of the mapping process. Pointer justification should be avoided in this case in order to minimize the impact on jitter.

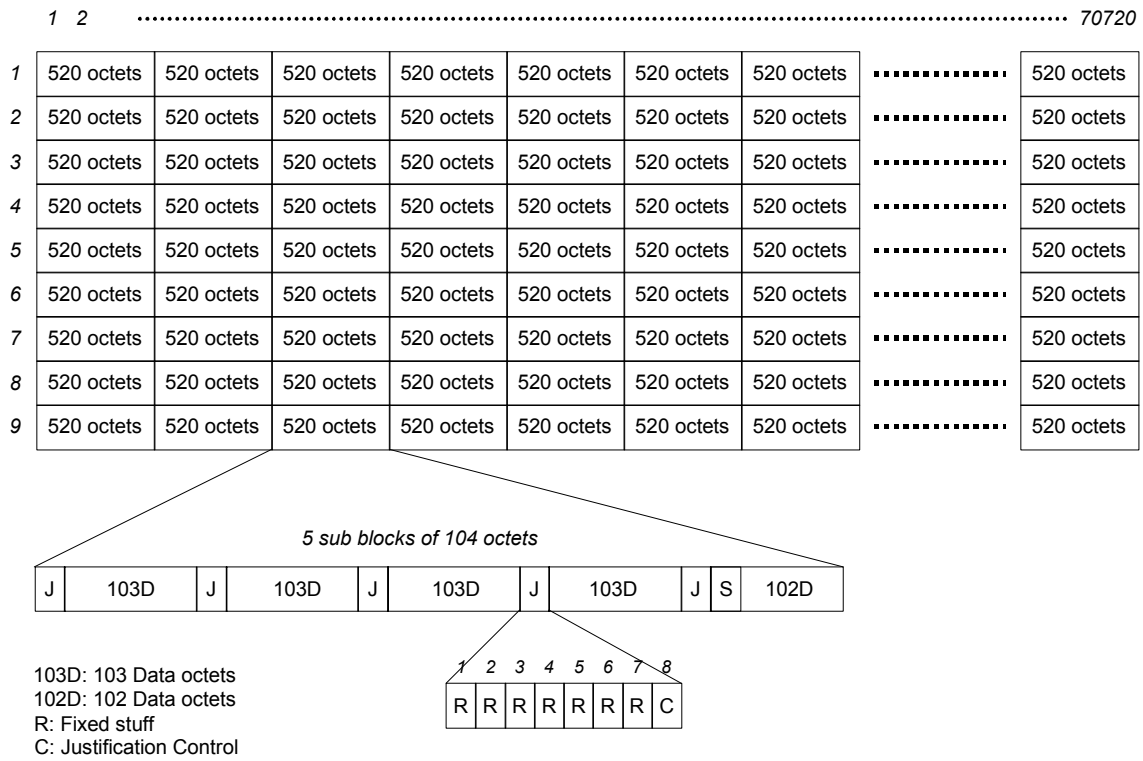


Figure A.1: Block structure for ODU3 mapping into C-4-272c

Figure A.2 details the mapping of ODU3 over the C-4-272c for transport through the TFI-5 system over 272 STS-3c / VC-4's: the ODU3 is mapped into a single C-4-272c and this concatenated structure is column disinterleaved and mapped into the 272 VC-4's. The 272 VC-4's generated in this way can be transported over any combination of TFI-5 links.

Figure A.3 details the demapping of an ODU3 from 272 VC-4's. The 272 C-4's are demapped from the 272 VC-4's (received from any combination of TFI-5 links) and column interleaved to obtain the C-4-272c. The ODU3 is then demapped from the C-4-272c.

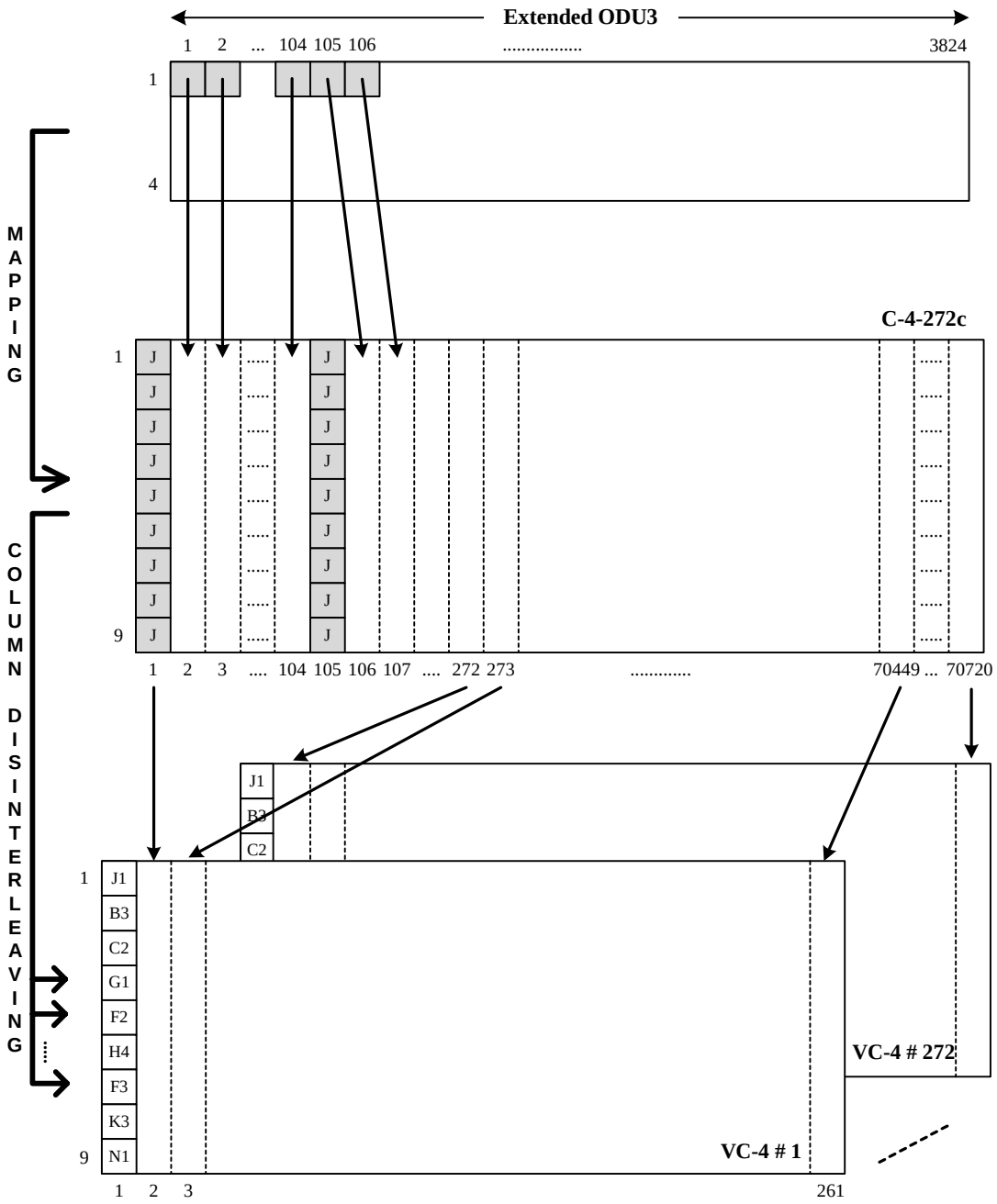


Figure A.2: Mapping of ODU3 over C-4-272c for transport over 272 VC-4's

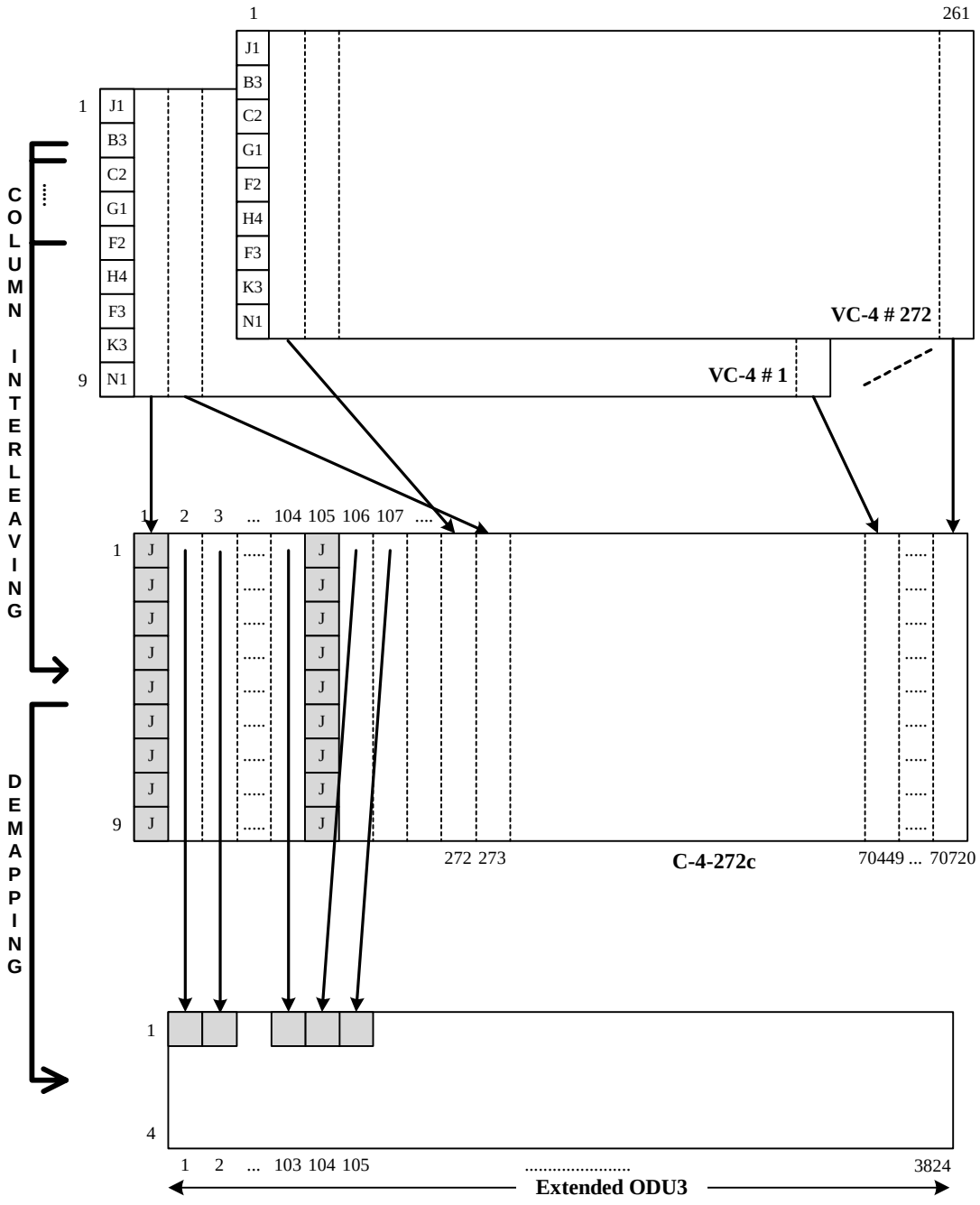


Figure A.3: Demapping of an ODU3 from a C-4-272c transported over 272 VC-4's

A.2 Mapping of 10GE LAN PHY

A simple way to transport an IEEE 10 GE LAN PHY signal [8] through a TFI-5 system is by mapping the 64B66B 10Gbps Ethernet bit stream (10GBASE-xR) into a C-4-70c and transporting the C-4-70c over 70 STS-3c / VC-4's. The mapping method is based on the ODU mapping into SONET/SDH as defined in [7].

Note that also a 10 GbE LAN PHY signal with 8B/10B line coding is defined (10GBASE-LX4). In order to map such a signal a 8B/10B to 64B/66B recoding is needed.

Table A.1 shows the structure used for mapping and the number of STS-3c/VC-4's required for transport of a 10GE LAN PHY signal and the mapping efficiency of the described method.

Client Signal	Nominal Bit Rate (Mb/Sec)	Mapped over	Transported using	Mapping Efficiency
10GE LAN PHY	10312.5	C-4-70c	70 VC-4's	98.37%

Table A.1: Mapping of 10GE LAN PHY: format and efficiency

Table A.2 shows the maximum and minimum client signal frequency deviation from the 10GE LAN PHY nominal frequency and the nominal justification ratio. Note that the bit rate tolerance of an 10 GE LAN PHY signal is only ±100ppm.

Client signal	Minimum frequency deviation from nominal	Maximum frequency deviation from nominal	Nominal Justification Ratio
10GE LAN PHY	-1041	913	0.532738095

Table A.2: Mapping of 10GELAN PHY: rate adaptation

The basic C-4-70c structure is comprised of 9 rows by 18200 (i.e. 70 x 260) columns. The 10GE LAN PHY signal is mapped into this C-4-70c with the following structure (see Figure A.4):

1. Each of the nine rows is partitioned into 35 blocks, consisting of 520 octets each.

2. In each block, one negative justification opportunity octet (S) and five justification control bits (C) are provided.

3. Each block is partitioned into 8 sub-blocks, consisting of 65 octets each.

    a. The first byte of each sub-block consists of either:

        i. A fixed stuff byte (R); or

        ii. A justification control byte (J), which consists o seven fixed stuff bits (bits R; bits 1 to 7) and a justification control bit (bit C, bit 8).

    b. The second byte of the last sub-block is a negative justification opportunity byte (S).

    e. The last 64 bytes of the first seven sub-blocks consist of data bytes (D).

    f. The last 63 bytes of the last sub-block consist of data bytes (D).

The set of five justification control bits (C) in every block is used to control the corresponding negative justification opportunity byte (S). CCCCC = 00000 indicates that the S byte is an information byte, whereas CCCCC = 11111 indicates that the S byte is a justification byte.

At the synchronizer all five C bits are set to the same value. Majority vote (3 out of 5) should be used to make the justification decision at the desynchronizer for protection against single and double bit errors in the C bits.

The value contained in the S byte when used as justification byte is all-ZERO's. The receiver is required to ignore the value contained in this byte whenever it is used as a justification byte.

CSI Code	Alarm/Condition
1111 1111	TFI-5 Link Loss of Signal
1111 1111	TFI-5 Link Loss of Frame
1111 1110	Software Force - Away
1111 1101	Software Local Fault Insert
1111 1100	Software Force-To
	PMD Loss of Signal
	PMA Loss of Synchronization
	PCS Loss of Block Lock
	PCS Remote Fault
	High Bit Error Rate
	Degraded Bit Error Rate
0000 0001	No Alarm
0000 0000	Reserved

Table A.3: : Client Status Indication (CSI) Coding for 10GE LAN PHY clients.

The value contained in the R bits and bytes is all-ZERO's. The receiver is required to ignore the value contained in these bits/bytes.

- The blank CSI code values are user programmable.
- Above each alarm/condition with a blank code point, there may be a user defined CSI alarm/condition entry. These may be used for augmenting the listed alarms/conditions with other simultaneously occurring alarms/conditions
- Generation of the CSI byte for alarms/conditions with blank code points are application dependent.
- See Section 10.2.2 for the Connectivity Monitoring (CM byte).

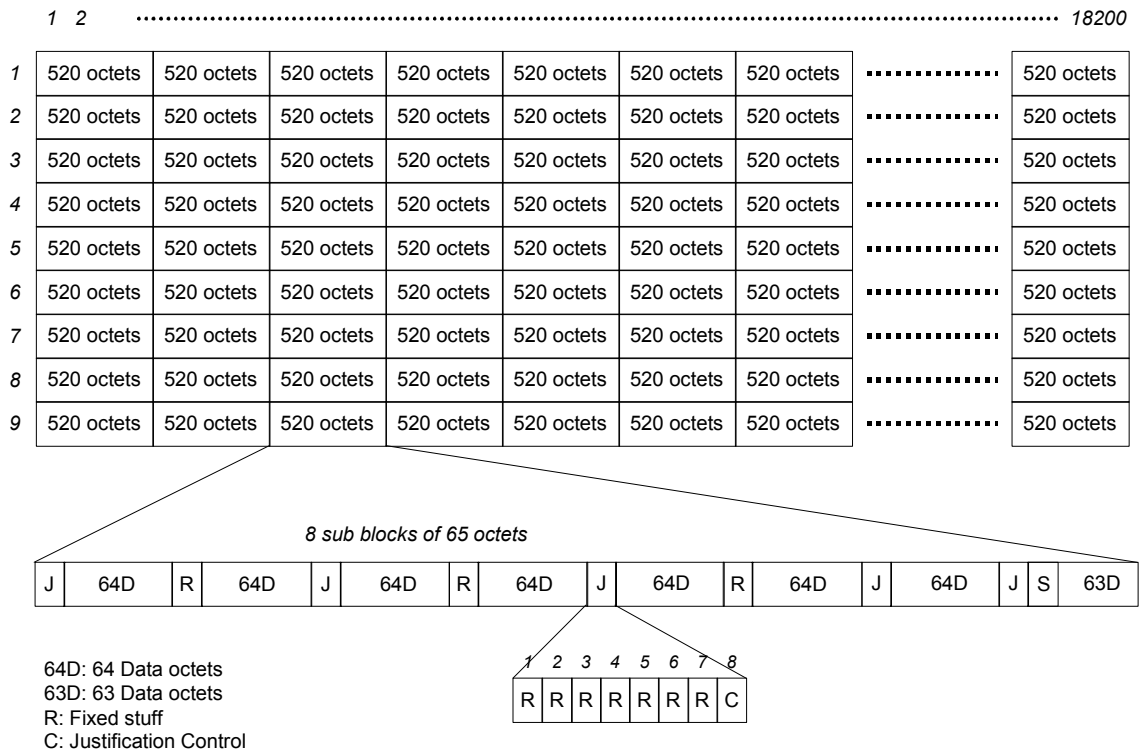


Figure A.4: Block structure for 10GE LAN PHY mapping into C-4-70c

Figure A.5 details the mapping of 10GE LAN PHY over the C-4-70c for transport through the TFI-5 system over 70 STS-3c / VC-4's: the 10 GE LAN PHY signal is mapped into a single C-4-70c and this concatenated structure is column disinterleaved and mapped into the 70 VC-4's. The 70 VC-4's generated in this way can be transported over any combination of TFI-5 links.

Figure A.6 details the demapping of 10GE LAN PHY from 70 VC-4's. The 70 C-4's are demapped from the 70 VC-4's (received from any combination of TFI-5 links) and column interleaved to obtain the C-4-70c. The 10GE LAN PHY signal is then demapped from the C-4-70c.

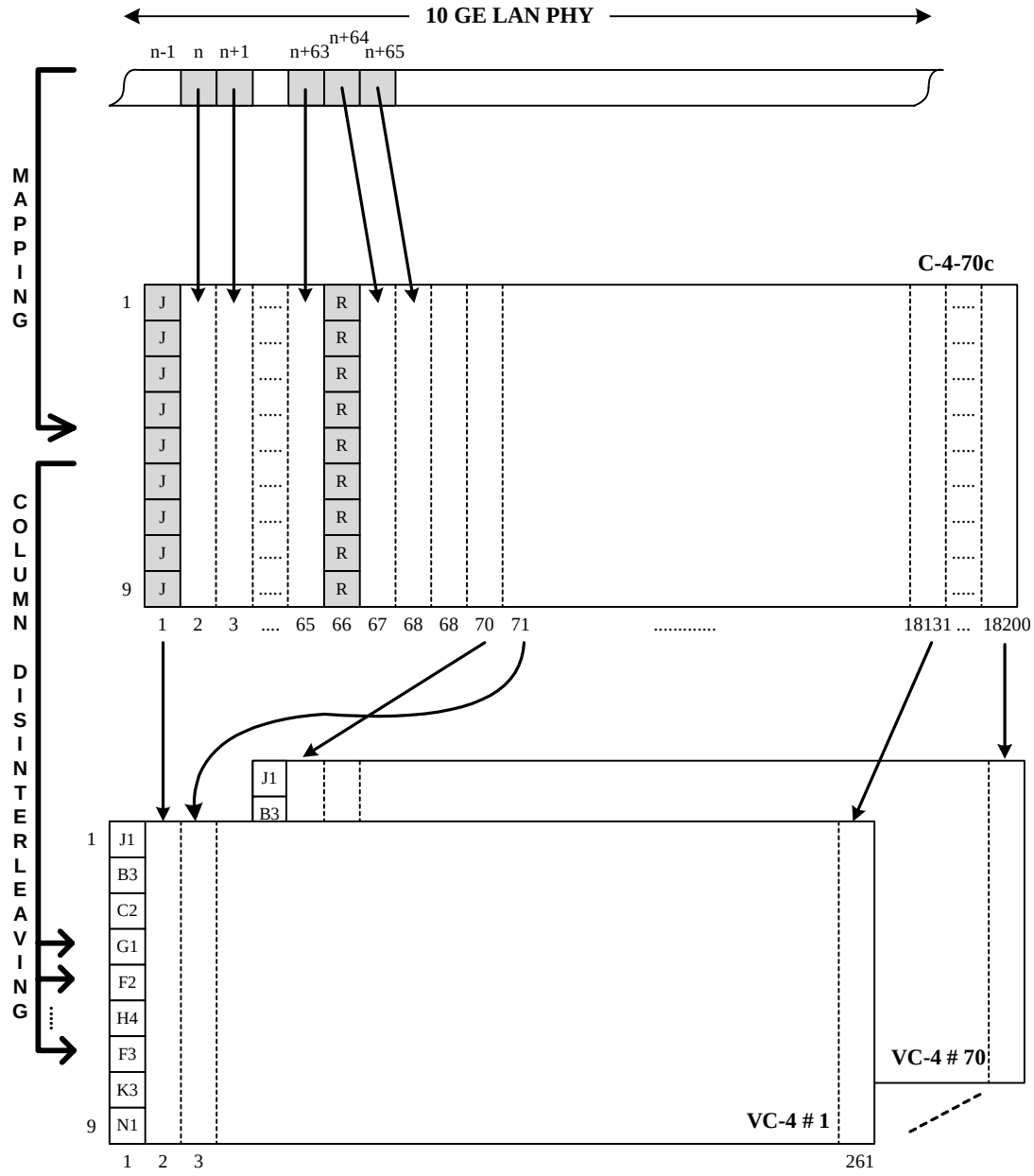


Figure A.5: Mapping of 10GE LAN PHY over C-4-70c for transport over 70 VC-4's

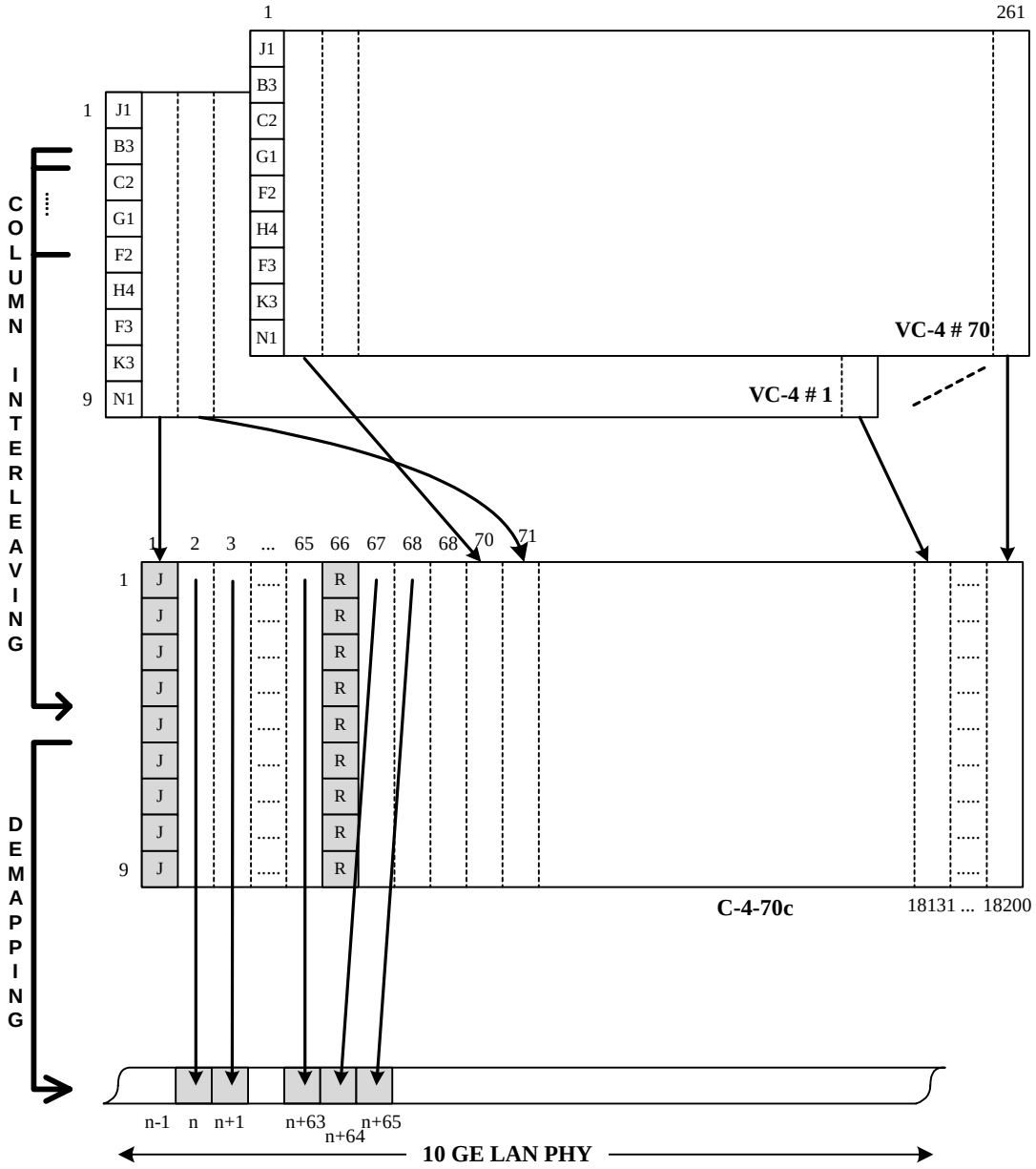


Figure A.6: Demapping of 10GE LAN PHY from a C-4-70c transported over 70 VC-4's

Appendix B: Jitter Notes

The following backplane physical assumptions for TFI-5 are used:

•Line -> Switch 9“+12“+9“ = 30”. For communications from a line card to a switch card, it is assumed that there are 9 inches of PCB trace on the line card, 12 inches on the FR-4.6 backplane, and another 9 inches on the switch card.•Line -> Line 3" 24" 3“ = 30”. For communications between two line cards, 3 inches are assumed on the line cards and 24 inches on the FR-4.6 backplane. The backplane is assumed to be composed of FR4-6 material, while the line and switch cards are assumed to contain FR4-2 material.Table B.1 shows a jitter budget for electrical intra-rack and electro-optical inter-rack applications. Entries with green highlights are presented in Section 11 and 12 as normative figures. The other entries are informative.

	Intra-rack (3.11Gbps)		
Test Point	DJ	RJ	TJ
TP1	0.170	0.180	0.350
TP1 to TP4	0.200	0.210	0.410
TP4	0.370	0.277	0.647

	Plenary Inter-rack (2.50 Gbps)			Plenary Inter-rack (3.11 Gbps)		
Test Point	DJ	RJ	TJ	DJ	RJ	TJ
TP1	0.120	0.140	0.260	0.120	0.140	0.260
TP1 to TP1.5	0.020	0.000	0.020	0.020	0.000	0.020
TP1.5	0.140	0.140	0.280	0.140	0.140	0.280
TP1.5 to TP2	0.120	0.170	0.290	0.120	0.200	0.320
TP2	0.260	0.220	0.480	0.260	0.244	0.504
TP2 to TP3	0.000	0.120	0.120	0.000	0.150	0.150
TP3	0.260	0.251	0.511	0.260	0.287	0.547
TP3 to TP3.5	0.088	0.190	0.278	0.110	0.230	0.340
TP3.5	0.348	0.315	0.663	0.370	0.367	0.737
TP3.5 to TP4	0.025	0.000	0.025	0.030	0.000	0.030
TP4	0.373	0.315	0.688	0.400	0.367	0.767

Table B.1: Jitter budget for electrical intra-rack and electro-optical inter-rack applications.

Appendix C Sample Application

C.1 STS-1 Cross-connect

In this informative annex, a SONET/SDH STS-1 cross-connect system is discussed as a typical application for TFI-5 links. The main function of an STS-1 cross-connect system is to take an arbitrary STS-1 from any ingress SONET/SDH fiber and place it on an arbitrary STS-1 of any egress fiber. Many systems also support multi-cast. In which case, an ingress STS-1 is routed to several egress STS-1's, possibly residing in multiple fibers. A typical cross-connect has switching bandwidth of 100 Gbps to 1 Tbps. Future systems are expected to be bigger. Thus, the switching fabric is shown to be constructed from several switching devices.

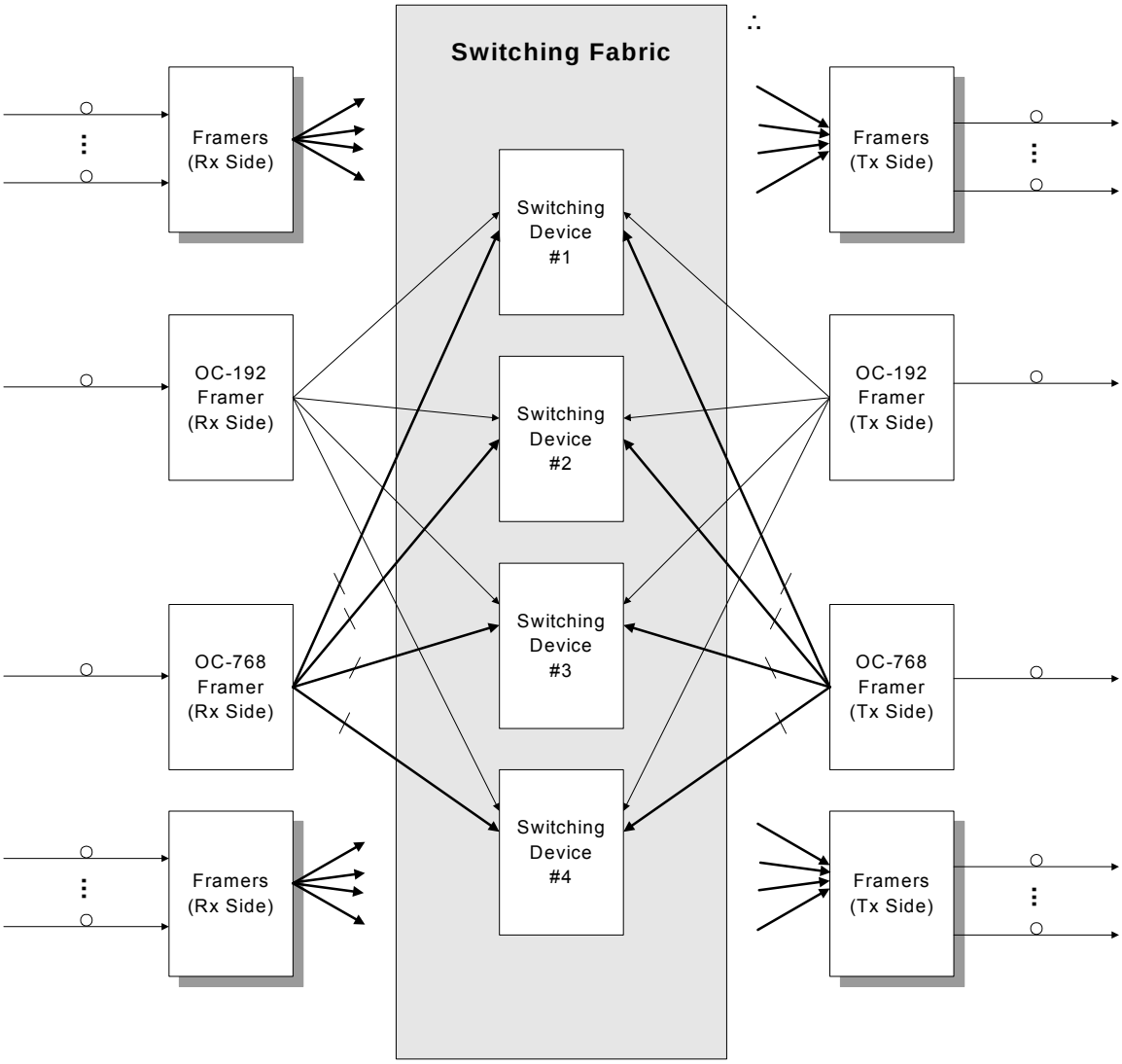


Figure C.1: STS-1 Cross-Connect Example

Figure C.1 above shows an example STS-1 cross-connect system. For clarity, the receive and transmit sections of the framers are drawn separately.

The connections of an OC-192 and an OC-768 framer are shown in detail. The switching fabric is shown to consist of 4 switching devices, as a single device is unlike to have sufficient bandwidth to satisfy system requirements.

Consider first the OC-192 framer. It sends 4 TFI-5 links towards the switching fabric and receives 4 links from the fabric. In order to minimize blocking, the links must be distributed to all 4 switching devices. If one concentrated all 4 framer links onto a single switching device, one would not be able to route between 2 framers unless they are both connected to the same switching device.

For systems that support multi-cast, it is necessary to balance which ingress STS-1 is sent to which switching device. Consider the example where STS-1's number 1 to 48 from the OC-192 framer is to be broadcast to all egress fibers. If one were to route all 48 STS-1's to the switching device #1, all data replication would occur inside that switching device. All the egress links of that switching device towards the transmit side of the framers would be consumed. The remaining ingress links of switching device #1 would unusable. One could either direct traffic away from switching device #1 or spread the multi-cast traffic over 4 TFI-5 links. Both solutions require flexible assignment of STS-1 to TFI-5 links.

The behavior of the OC-768 framer is very much analogous to that of the OC-192 framer. The only difference is that it sources a set 4 of links to each switching device and sinks a set of 4 links from each switching device. Load balancing applies among the 4 sets of links. Depending on the properties of the switching device, there may not be any requirement to load balance within each set of links.

Each switching device terminates a large number of ingress TFI-5 links and sources a large number of egress TFI-5 links. Being a TDM element, the switching device is synchronous. It requires that all the ingress links to be frame aligned and frequency locked to a common reference. One can see from Figure C.1, some ingress links originate from the same framer but the majority originates from many different framers. It is therefore necessary to limit skew, not just between links from a single framer, but also between links from different framers.

A similar situation also applies to the egress links between the switching devices and the framers. Each framer terminates links from all the switching devices. Processing can be greatly simplified if all the links are frequency locked and frame aligned. Otherwise, large de-skew FIFO's would be required and delays would become undesirably large. Thus, TFI-5 requires that all links within a system to be frequency locked and frame aligned.

Appendix D: Inter-Connect Characteristics

Connector Impedance

The recommended characteristic differential impedance of the connector(s) is to be 100Ω +/- 20%.

Characteristic Impedance

The recommended characteristic differential impedance of the channel (including any connectors) is to be 100Ω with a return loss better than –10dB from near DC to 0.75 times the baud rate. The recommended single-ended impedance is to be 50Ω with a return loss better than –6dB from near DC to 0.75 times the baud rate.

Channel Model

Inter-connect Loss

This specification is intended as a point-to-point interface of 0 up to 75cm between integrated circuits using controlled impedance traces on low-cost printed circuit boards (PCBs). A simple model for PCB loss is given below [26].

$$Att = \alpha_{metal} + \alpha_{dielectric} = \frac{4.34}{2.54}\left(\frac{R_{DC} + R_{AC}}{Zo} + G_L * Zo\right)$$

$$Att = \frac{-4.34}{2.54 * Zo} * \left(\frac{\rho}{W}\left(\frac{1}{t} + \frac{0.75}{63\mu}\sqrt{f}\right)\right) - \frac{2.3}{2.54} * f * \tan(\delta) * \sqrt{\varepsilon r}$$

Where **Zo** is the characteristic impedance, **W** is the track width, **tan(δ)** is the loss tan, **t** is the track thickness, **f** is the frequency in GHz, ρ is the sheet resistively, ε_r is the relative permittivity and **Att** is in dB/cm.

Table D.1 gives the attenuation for the PCB (does not include non-ideal vias or connectors) for the case of: Zo=50Ω, W=8mils and t=1oz (30μm).

	FR4-2	FR4-6	FR4-13	Units
Loss Tan [27]	0.027	0.025	0.016	
εr [27]	4.2	4.0	3.7	
Loss per cm (@1.6GHz)	0.0850	0.0773	0.0494	dB/cm
Loss @ 20cm (@1.6GHz)	1.70	1.55	0.99	dB
Loss @ 75cm (@1.6GHz)	6.38	5.80	3.71	dB
Loss @ 1m (@1.6GHz)	8.50	7.73	4.94	dB
Loss per cm (@3.2GHz)	0.1658	0.1504	0.0947	dB/cm
Loss @ 20cm (@3.2GHz)	3.32	3.01	1.89	dB
Loss @ 75cm (@3.2GHz)	12.44	11.28	7.10	dB
Loss @ 1m (@3.2GHz)	16.58	15.04	9.47	dB
Loss per cm (@5.5GHz)	0.2817	0.2552	0.1594	dB/cm
Loss @ 20cm (@5.5GHz)	5.63	5.10	3.19	dB
Loss @ 75cm (@5.5GHz)	21.13	19.14	11.96	dB
Loss @ 1m (@5.5GHz)	28.17	25.52	15.94	dB

Table D.1 PCB Effects

Now one has to add in the losses for vias and connectors. At baud rate divided by 2 typically one adds about 1dB per connector (assumes a “good” connector for that frequency of operation).

Also at baud rate divided by 2 one typically adds 0 to 6 dB for non-ideal vias and reflections. The value depends on the overall length, the type of interconnect (micro-strip line or strip line, strip line typically being worse), return loss of Rx/Tx and transmission line, etc. Of note, the value is typically higher for shorter lengths (as reflections will not be reduced as much).

Another popular way to spec the channel loss is to have an average or worse case “curve” fit to several real channels. This method includes effects of real vias and connectors (hence should give curves that are worse than the PCB model above). Both methods are useful (the PCB model to show the “best” case, and the curve fit model to show “some real design cases”). This method typically uses the equation below:

$$Att = -20 * \log(e) * \left(a_1 * \sqrt{f} + a_2 * f + a_3 * f^2\right)$$

Where ***f*** is frequency in Hz, $\mathbf{a_1}$, $\mathbf{a_2}$, & $\mathbf{a_3}$ are the curve fit coefficients and **Att** is in dB. Table D.2 gives some examples of these coefficients. Figure D.1 shows various channel models along with the PCB model and a real 75cm backplane (with 5cm paddle cards on both ends).

	a_1	a_2	a_3
XAUI [10] (50cm)	6.5e-6	2.0e-10	3.3e-20
75cm [29] “Worse”	6.5e-6	3.9e-10	5.0e-20
75cm [29] “Typical”	6.0e-6	3.9e-10	3.5e-20

Table D.2 Curve fitting Coefficients

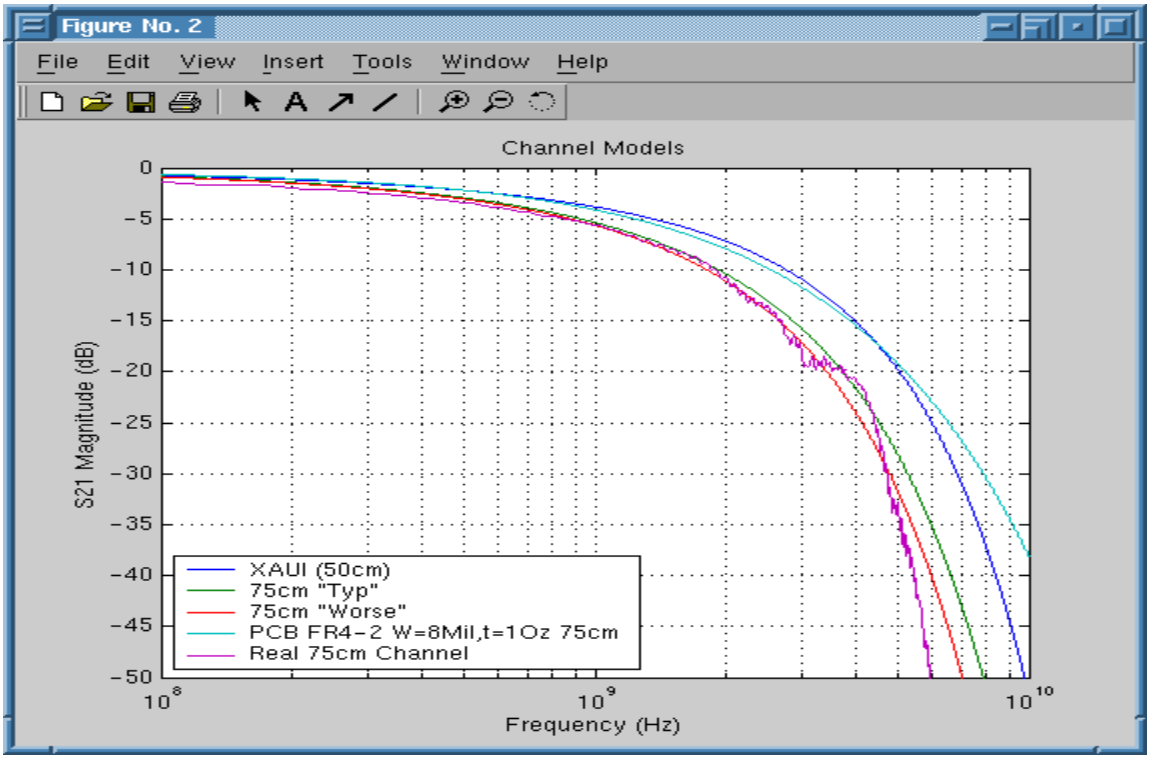


Figure D.1 Channel Models

Appendix E: Cross Talk

Cross talk arises from coupling within the connectors, on the PCB, the package and the die. Cross talk can be categorized as either Near-End or Far-End Cross talk (NEXT and FEXT). In either of these categories, the amount of cross talk is dependent upon signal amplitudes, signal spectrum, and trace/cable length. There can be many aggressor channels onto one victim channel, however typically only a few are dominant.

A simplistic cross talk model (i.e. summation of all aggressor channels onto the one victim channel) would have a transfer function that rises at 20dB/dec from DC to some frequency Fz, and then flattens out till frequency Fp where it drops off. The slope at which it drops off is ill defined, but can be assumed to be either 20dB/dec or 0dB/dec (i.e. does not drop off) for modeling ease. The peak value of the transfer function is channel specific.

This standard assumes that the dominant cross talk can come from aggressors other than the transmitter associated with the receiver.

Jitter caused by cross talk is bounded DJ, but can look like quite gaussian, and hence most measuring equipment will indicate it as RJ (thus multiplying the 1 sigma value by 14, hence over estimating the amount of jitter).

Appendix F: Terms and Definitions Glossary

Here is a glossary of some acronyms used in the implementation agreement:

AISC-P	Alarm Indication Signal Concatenation Indication—Path Layer
AIS-L	Alarm Indication Signal Line Layer
AIS-P	Alarm Indication Signal Path Layer
EXC-MS	Excessive Bit Error—Multiplexed Section Layer
EXC-P	Excessive Bit Error—Path Layer
LOF	Loss of Frame
LOM	Loss of MultiFrame
LOS	Loss of Signal
OOF	Out of Frame
PDI	Path Defect Indication
PLM	Payload Label Mismatch
SD-L	Signal Degrade—Line Layer
SD-P	Signal Degrade—Path Layer
SF-L	Signal Fail—Line Layer
TIM-S	Trace Identifier Mismatch—Section Layer
UNEQ	Unequipped
AC	Alternating current
AIS	Alarm indication signal
AU	Administrative unit
BER	Bit error ratio
C-N	Container of level N
CID	Connection identifier
CM	Connectivity monitoring
DC	Direct current
FDI	Forward defect indication
GE	Gigabit Ethernet
INF	In frame
LAN	Local area network
OC-N	Optical carrier of level N
ODUN	Optical channel data unit of level N
OOF	Out of Frame
OTN	Optical Transport Network
PCB	Printed circuit board
PHY	Physical interface
CSI	Client Status Indication
SDH	Synchronous Digital Hierarchy
SOH	Section overhead
SONET	Synchronous Optical Network
SPE	Synchronous payload envelop
SPI-N	System packet interface of level N
STM-N	Synchronous transport module of level N
STS-N	Synchronous transport signal of level N

TDM	Time division multiplexing
TOH	Transport overhead
VC-N	Virtual container of level N
VCSEL	Vertical cavity
WAN	Wide area network

Correlated Wander
: Components of wander that are common across all applicable in band signals.

Relative Wander
: Components of wander that are uncorrelated between any two in band signals (SxI-5 Figure 4.1)

Total Wander
: The sum of the correlated and uncorrelated wander. (See SxI-5 Figure 4,2)

Uncorrelated Wander
: Components of wander that are not correlated across all applicable in band signals.

Wander
: The peak to peak variation in the phase of a signal(clock or data) after filtering the phase with a single pole low pass filter with the –3db point at the wander corner frequency. Wander does not include skew.

Skew
: The constant portion of the difference in the arrival time between the data of any two in-band signals.

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