Implementation Agreement for Micro Intradyne Coherent Receivers

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ABSTRACT: Implementation agreement for a micro intradyne coherent receiver (ICR) – Revision 02.0, with additions addressing higher bandwidth / higher symbol rate applications.

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Document Revision History

Document	Date	Revisions/Comments
OIF-DPC-MRX-01.0	March 31, 2015	First release
OIF-DPC-MRX-02.0	June 21, 2017	Second release, with following edits: • Updated introduction to make text symbol rate / data rate agnostic; • Re-ordered paragraphs to improve document flow; • Moved electro-optical characteristics from informative appendix to normative section; • Introduced three classes of micro-ICR (Class 20, 30 and 40), corresponding to devices having notional S_{21} bandwidths of 20GHz, 30GHz, and 40GHz, respectively; • Added target masks for S_{21} optical-to-electrical transfer function and S_{22} electrical return loss frequency responses;

1 Introduction

This document details an Implementation Agreement for a Micro-Intradyne Coherent Receiver (µICR) targeting modulation and data-rate agnostic coherent applications having nominal symbol rates up to 64Gbaud. The IA aims to identify and specify the common features and properties of coherent receivers to enable them to broadly meet the needs of current and future coherent systems.

The µICR Implementation Agreement defines the following: (1) Required functionality; (2) High speed electrical interfaces; (3) Low speed electrical interfaces; (4) Environmental and operating characteristics; (5) Electro-optical characteristics; (6) Mechanical requirements. Additional informative electro-optical specifications are also included in Appendix B.

Both a primary and alternative electro-mechanical form factor are defined in this revision of the µICR IA. The primary electro-mechanical form factor (Type 1) uses a surface mount configuration. The alternative electro-mechanical form factor (Type 2) employs flexible PCBs for the DC and RF I/O interfaces. The Type 2 form factor can allow for the direct connection of the µICR hot zone to the heat sinking surface in the use-case of a pluggable coherent module. Differences between the Type 1 and Type 2 form factors are highlighted where appropriate, otherwise common characteristics are required for the two form factors.

The IA also defines an option for a low speed electrical interface that incorporates an SPI bus to control the Trans-Impedance Amplifiers (TIAs) in the µICR. The SPI enabled low speed interface is equally applicable to either the Type 1 and Type 2 electro-mechanical form-factors. The choice of a combination of the package form factor and whether the low speed electrical interface incorporates an SPI bus will be specific to the application and/or µICR customer preference.

The IA does not define the technologies used to implement the IA, nor the expected optical transmission performance of coherent systems using receivers conforming to the IA.

2 Functionality

The functional blocks required to implement a coherent receiver are shown in Figure 2-1. A μICR that meets the objectives of the IA contains the functionality shown within the dashed line box in Figure 2-1.

A μICR shall provide at a minimum the following functionality:

1. A Signal input fiber that shall be Single Mode Fiber (SMF).
2. A Local Oscillator (LO) input fiber that shall be Polarization Maintaining Single Mode Fiber (PM-SMF).
3. A polarization splitting element, separating the input Signal light into two orthogonal polarizations, with each polarization delivered to a 90 degree hybrid mixer.
4. A polarization maintaining power splitter or polarization splitting element, splitting the local oscillator input power equally and delivering it to the two 90 degree hybrid mixers.
5. Two (2) 90 degree hybrid mixers with differential optical outputs.
6. Eight (8) photo-detectors comprised of 4 sets of differential detectors.
7. Four (4) linear trans-impedance amplifiers providing differential AC coupled RF output signals [XI, XQ, YI, YQ.].

A μICR *may* also contain the following optical functionality:

8. Optical power tap(s) and monitor photodiode(s) in the Signal input path either before the signal polarization splitting element or in each path after the splitting element.
9. A variable optical attenuator in the Signal input path either before the signal polarization splitting element or in each path after the splitting element.

X (X-Pol) and Y (Y-Pol) indicate a pair of mutually orthogonal polarizations of any orientation, and I and Q are mutually orthogonal phase channels in each polarization. As shown in Figure 2-1 the μICR therefore has 4 polarization-phase RF output channels labeled as XI, XQ, YI, YQ.

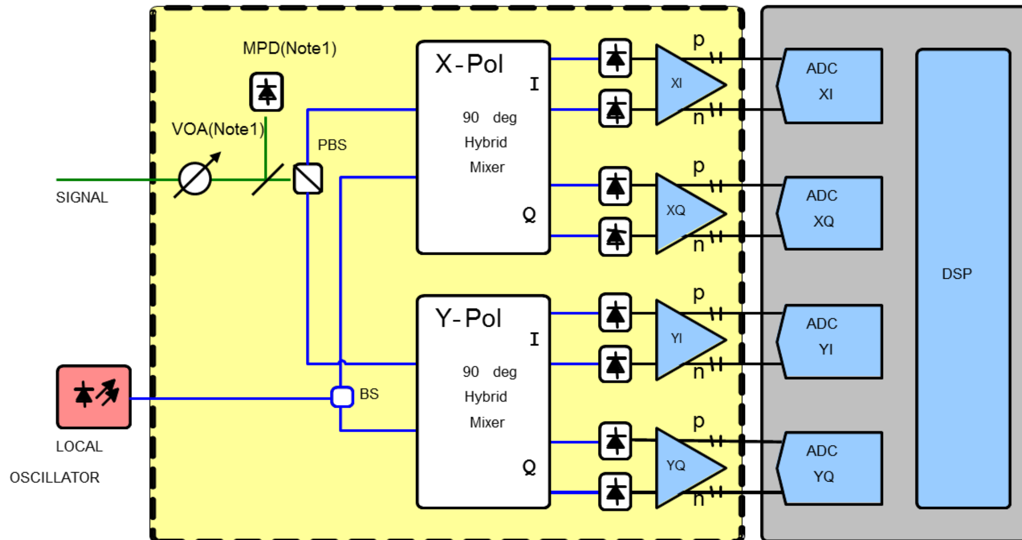


Figure 2-1 Functional blocks in a coherent receiver.

Notes:

1. VOA and MPD are optional. One configuration for the order of the VOA and MPD is shown. The configuration with the MPD followed by the VOA is an equally acceptable configuration. Configurations having VOAs and/or MPDs after the polarization beam splitter (one VOA/MPD per polarization) are also considered acceptable implementations.
2. The yellow area enclosed by the dashed line indicates the µICR functionality specified in the IA.

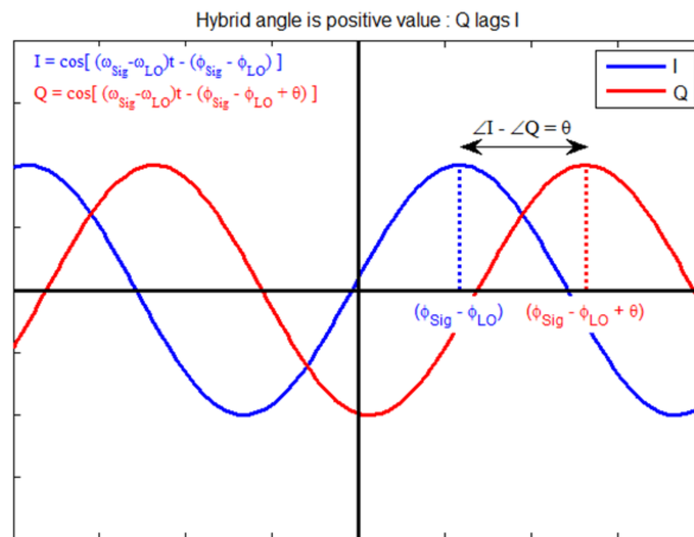


Figure 2-2 Definition of hybrid angle.

The phase relationship between I and Q outputs is established by the heterodyne technique with the frequency of the Signal input to the receiver greater than the frequency of the LO input. Under this condition, when the I and Q output waveforms are observed in the time domain, the Q channel *lags* the I Channel by nominally +90 degrees, as shown in Figure 2-2.

Channel outputs 'p' and 'n' are the complementary outputs for each polarization-phase channel and are defined such that the output voltage for 'p' increases as the Signal and Local Oscillator approach the in-phase condition to form constructive interference, and the output voltage for 'n' decreases under the same conditions.

The TIAs in the µICR function enable multiple signal monitors and control methods. The most notable TIA control selection is between automatic or manual gain control operating mode (AGC or MGC). TIAs can support AGC only, MGC only, or both – all are valid implementations. The TIAs may also facilitate a bandwidth equalization function and provide various input signal strength and/or output level monitors (PI). In the AGC operating mode there is a RF output level adjust control (Output Adjust, OA) available and in the MGC operating mode an external signal (Gain Adjust, GA) is used to control the gain of each differential amplifier.

3 High Speed Electrical Interface

3.1 High Speed Electrical Interface in the Type 1 Mechanical Form Factor

The high speed electrical output interface for a Type 1 µICR form-factor uses surface mounted pins in a differential co-planar waveguide arrangement (GSSG), with shared ground pins. The pin definitions and pitches shall be as detailed in Table 3-1, Table 3-2, and Figure 3-1. It is noted that alternate configurations for the differential signals shown in Figure 3-1 are acceptable.

All allowable channel mappings are enumerated in Table 3-3. The pin configuration shown in Figure 3-1 corresponds to mapping [0,0,0]. Each mapping is specified by three designations: [X:Y ; I,Q ; p/n], where a ":" is used to separate X&Y, a "," is used to separate I&Q, and a "/" is used to separate p&n. In Table 3-3 red text shows where the mapping flips occur relative to the 1st row in each group. It is important to highlight that Table 3-3 *does not* allow interleaving of the channels by polarization since this would add a non-essential level of complexity to the digital signal processing.

Parameter	Value	Notes
Interface type	Differential	
Channel number	4	
Channel configuration	G-S-S-G	Per Figure 3-1
Signal line coupling	AC	
Signal line impedance	100 Ohm Differential	
Channel pin-out	XI XQ YI YQ	Per Figure 3-1
Differential pin-out	Signal Complimentary Signal	p n

Table 3-1 High speed electrical interface description.

Parameter	Symbol	Min	Typ	Max	Units
Lead pitch	A		0.8		mm
Lead length (referenced from outside wall of package, as defined by dimension LP2 in Section 7)	B	1.5	2.0	2.5	mm
Signal lead width	C	0.1	0.2	0.3	mm
Ground lead width	D	0.1	0.2	0.3	mm
Channel pitch	E		2.4		mm
Signal to complimentary signal pitch	F		0.8		mm

Table 3-2 Type 1 high speed electrical interface dimensions.

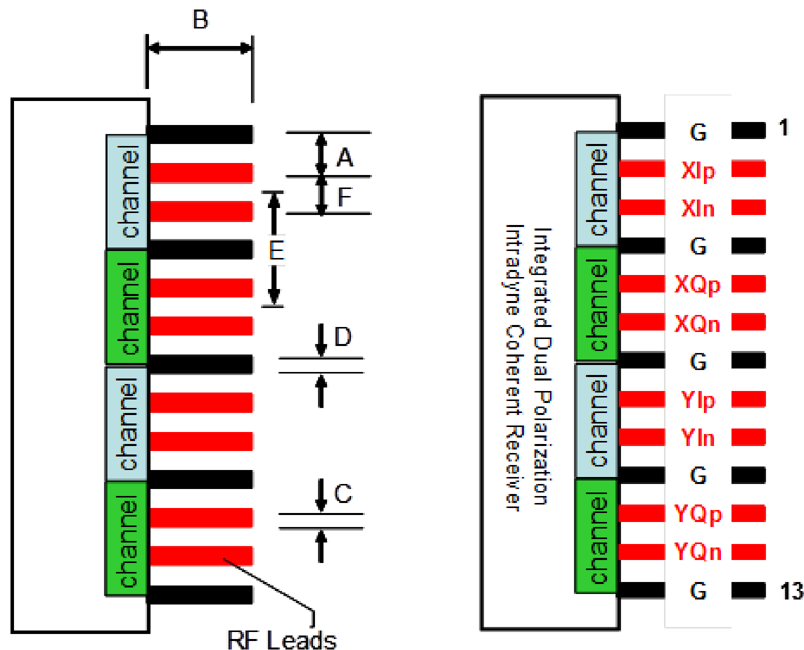


Figure 3-1 High speed electrical interface definition.

Mapping	X:Y	I,Q	p/n	Notes
[0,x,x]	X:Y			Pol. cannot be interleaved
[1,x,x]	Y:X			
[x,0,x]		I,Q:I,Q		Same across Pol.
[x,1,x]		Q,I:Q,I		
[x,2,x]		I,Q:Q,I		Flip across Pol.
[x,3,x]		Q,I:I,Q		
[x,x,0]			p/n,p/n:p/n,p/n	Same across Pol. and I,Q
[x,x,1]			n/p,n/p:n/p,n/p	
[x,x,2]			p/n,p/n:n/p,n/p	Flip across Pol.
[x,x,3]			n/p,n/p:p/n,p/n	
[x,x,4]			p/n,n/p:p/n,n/p	Flip across I,Q
[x,x,5]			n/p,p/n:n/p,p/n	
[x,x,6]			p/n,n/p:n/p,p/n	Flip across Pol. and I,Q
[x,x,7]			n/p,p/n:p/n,n/p	

Table 3-3 Allowable channel mappings for the µICR high speed electrical interface.

3.2 High Speed Electrical Interface in the Type 2 Mechanical Form Factor

The high speed electrical interface for the Type 2 form factor is realized using an RF flexible PCB. This allows for a customized RF connection between a vendor-specific interface on the µICR package and a customer-specific interface on the host PCB.

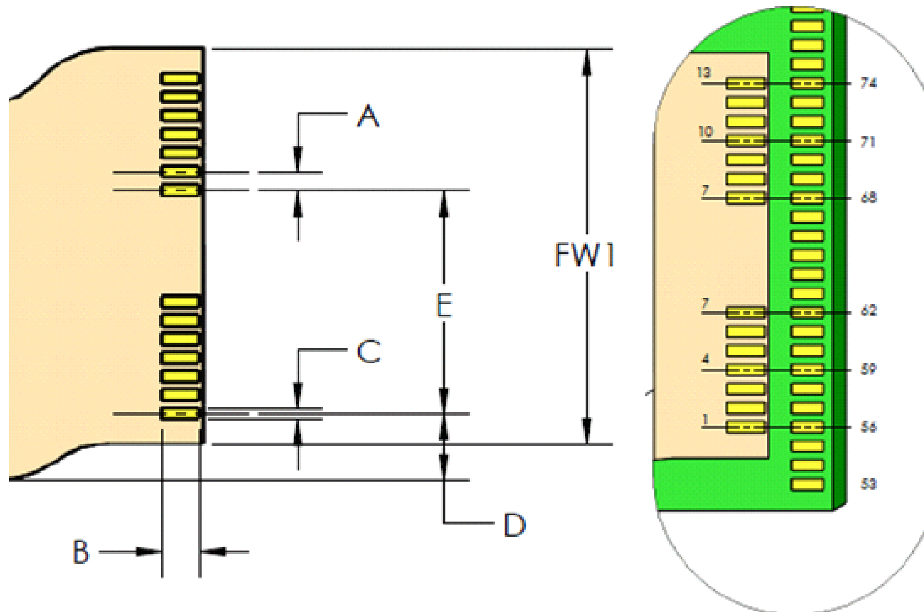


Figure 3-2 High speed flexible PCB interface for the Type 2 mechanical form factor enabling adaption to the CFP2-ACO module environment.

In one key example, the customer interface for the flexible PCB matches the pitch of a CFP2 connector as shown in Figure 3-2. Numerical values for the dimensions in Figure 3-2 are given in Table 7-2 and Table 7-3.

4 Low Speed Electrical Interface

4.1 Low Speed Electrical Interface in the Type 1 Mechanical Form Factor

The low speed electrical connections for the Type 1 form factor are provided through 34 pins, located on both sides of the package, and numbered as shown in Table 4-1. Note that unused pins on the interface are not required to be present.

The pin pitch shall be nominally 0.8 mm.

The low speed electrical interface pin functionality is specified in Table 4-1. Note that an equally valid alternative low speed interface pin definition implemented using an SPI bus is detailed in Section 8.

The photocurrent of each channel, or a representative equivalent quantity, shall be measurable.

Pin#	Symbol	Description		Pin#	Symbol	Description
1	RFU	Reserved for future use[4]		34	RFU	Reserved for future use[4]
2	RFU	Reserved for future use[4]		33	RFU	Reserved for future use[4]
3	MGC/AGC	MGC/AGC selection (optional)		32	SD	Shutdown (optional)
4	MPD-C	Monitor diode cathode (optional)[3]		31	VOA1	VOA1 Adjust voltage (optional)[2]
5	MPD-A	Monitor diode anode (optional)[3]		30	VOA2	VOA2 Adjust voltage (optional)[2]
6	PD-YI	Photodiode bias voltage YI[1]		29	PD-XQ	Photodiode bias voltage XQ[1]
7	PD-YI	Photodiode bias voltage YI[1]		28	PD-XQ	Photodiode bias voltage XQ[1]
8	PD-YQ	Photodiode bias voltage YQ[1]		27	PD-XI	Photodiode bias voltage XI[1]
9	PD-YQ	Photodiode bias voltage YQ[1]		26	PD-XI	Photodiode bias voltage XI[1]
10	PI-YI	Peak indicator YI		25	PI-XQ	Peak indicator XQ
11	GA-YI	Gain adjust YI		24	GA-XQ	Gain adjust XQ
12	OA-YI	Output amplitude adjust YI		23	OA-XQ	Output amplitude adjust XQ
13	VCC-Y	Supply voltage amplifier Y		22	VCC-X	Supply voltage amplifier X
14	GND	Ground Reference		21	GND	Ground Reference
15	OA-YQ	Output amplitude adjust YQ		20	OA-XI	Output amplitude adjust XI
16	GA-YQ	Gain adjust YQ		19	GA-XI	Gain adjust XI
17	PI-YQ	Peak Indicator YQ		18	PI-XI	Peak Indicator XI

Table 4-1 Low speed electrical interface definition.

Notes:

1. PD-YI, PD-YQ, PD-XI, PD-XQ are each assigned two pins where either:
    a. Each one of the two pins independently supplies the bias voltage for one of the two differential photodiodes in the labeled Polarization / Phase channel; or
    b. The first of the two pins (6, 8, 27, 29) is connected to both of the differential photodiodes for the labeled Polarization / Phase channel and the other pin (7, 9, 26, 28) is not connected within the µICR.
2. Pins 31 and 30 (VOA1 and VOA2) shall not be connected internally to ground. If separate VOA functions in the X- and Y-polarization channels are implemented, then the X channel shall be controlled by pin 31 (VOA1) and the Y channel shall be controlled by pin 30 (VOA2); both then being referenced to GND.
3. If independent monitor PDs are provided for the X- and Y-polarizations, the cathode of the X-polarization MPD shall be connected to pin 4 (MPD-C); the anode of the X-polarization MPD shall be connected to pin 5 (MPD-A); the cathode of the Y-polarization MPD shall be connected to pin 4 (MPD-C); and the anode of the Y-polarization MPD

shall be connected to GND. Internal circuitry providing equivalent functionality is acceptable.

4. Bandwidth Adjust controls – if available – should be present on pins 1, 2, 33, and 34 (marked as Reserved for Future Use). If only two pins are used for bandwidth control, the preference is to use pins 2 and 33.

4.2 Low Speed Electrical Interface in the Type 2 Mechanical Form Factor

The low speed interface for the Type 2 form factor is provided by a 34 pad flexible PCB connected to one side of the package body. The package interface is vendor-specific. The 34 pads on the host PCB are arranged in two rows of 17 pads as illustrated in Figure 4-1. Dimensional detail is provided in Figure 7-4 and Figure 7-5.

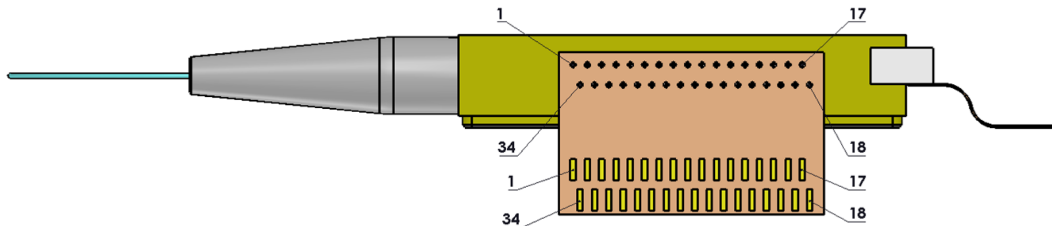


Figure 4-1 Low speed electrical interface in the Type 2 form factor.

The low speed electrical interface pin functionality is identical to the Type 1 implementation as specified in Table 4-1. Note that an equally valid alternative low speed interface pin definition implemented using an SPI bus is detailed in Section 8.

5 Environmental and Operating Characteristics

Basic operating characteristics are listed in Table 5-1.

Parameter		Unit	Min	Typ	Max	Note
Operating frequency	C-band	THz	191.35		196.20	1
	L-band		186.00		191.50	
TIA supply voltage		V	3.14	3.3	3.47	
Photodiode bias voltage	Option 3.3	V	3.135	3.3	3.465	2
	Option 5.0		4.75	5.0	5.25	
Monitor photodiode bias voltage	Option 3.3	V	3.135	3.3	3.465	2
	Option 5.0		4.75	5.0	5.25	
VOA control voltage (optional)		V	0		9	3
Operating temperature	Standard	°C	-5		75	4
	Preferred		-5		80	
Operating humidity (non-condensing)		%RH	5		85	

Table 5-1 Operating characteristics.

Notes:
1. Minimum supported range. At least one of the two frequency bands shall be supported.
2. Vendor shall state which Bias Voltage Option or Options are allowed, both for Signal Photodiodes and Monitor Photodiodes.
3. The VOA shall be of type “normally bright”.
4. The operating temperature is defined as the minimum/maximum of the µICR case “hot zone” surface temperature.

6 Electro-Optical Characteristics (Normative)

In this revision of the IA, electro-optical (EO) characteristics are provided for 3 Classes of µICR (Class 20, 30 and 40), corresponding to devices having notional S_{21} bandwidths of 20GHz, 30GHz, and 40GHz, respectively.

General EO characteristics common to all 3 Classes of µICR are given in Section 6.1. The RF frequency response specifications specific to each Class of µICR are given in Section 6.2. Other *Informative* EO characteristics for µICRs are given in Appendix 11.

Revision 1.0 of the µICR IA contained only *informative* EO specifications for a device with a notional 20GHz S_{21} bandwidth. Implementations of a µICR conforming to revision 1.0 and so identified, but not meeting all of the requirements presented herein, are still considered valid µICR implementations.

6.1 General Electro-Optical Characteristics

Parameter		Unit	Min	Typ	Max	Note
Operating signal power		dBm	-18	-10	0	
Local oscillator power		dBm			16	1
Maximum differential output swing		mVpp	700			2
Minimum differential output swing		mVpp			300	2
DC common mode rejection ratio ($CMRR_{DC}$)	Sig to I&Q	dBe			-20	3
	LO to I&Q				-16	
RF common mode rejection ratio ($CMRR_{RF}$)	Sig to I&Q	dBe			-16	3, 4
	LO to I&Q				-14	
Low frequency cut-off		MHz			1	5
Phase error		°	-7.5		+7.5	6
Optical reflectance		dB			-27	7
Skew between complimentary signals within a channel (informative)		ps			1	
Channel skew		ps			50	8
X/Y skew variation		ps			3.0	9
I/Q skew variation	Class 20	ps			2.0	10
	Class 30				1.5	
	Class 40				1.0	

Table 6-1 Electro-optic characteristics (normative).

Notes:

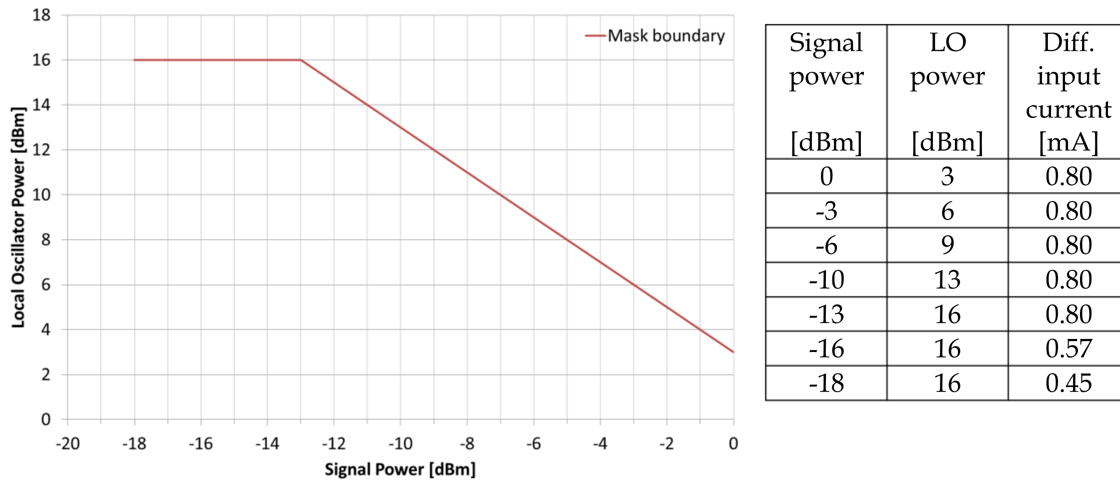
1. At high signal powers, the maximum desired local oscillator power is limited by the maximum TIA differential input current for linear operation. Figure 6-1 provides an informative example calculation for the allowed LO power as a function of the input Signal. In implementations with a VOA in the Signal path, the Signal power can be attenuated such that no adjustment to the LO power is required.

2. Peak to peak, differential, AC coupled output amplitude that can be achieved by controlling the output adjust (OA) in AGC mode, given sufficiently strong input Signal and LO powers.
3. CMRR = $20 \cdot \log(|\Delta I| / \sum I)$, where ΔI is the difference in photocurrent between the PDs in a differential pair (XI, XQ, YI, or YQ) and ∑I is the sum of the photocurrents from the PDs in the same PD pair. Note CMRR may not be directly measureable by the customer if no individual PD (p,n) bias pins are available on the low speed electrical interface.
4. RF CMRR is measured at 20GHz, 30GHz, and 40GHz for Class 20, 30, and 40 µICRs, respectively. The single-port rejection ratio (SPRR) measurement technique can be used to provide a suitable representation of the RF CMRR. The limits for Class 30 and 40 µICRs may be revised in a future revision of the document as more component and system level performance data becomes available.
5. AC coupled.
6. Between XI and XQ and between YI and YQ.
7. Signal and LO ports. Per ITU-T G.959.1
8. Time difference between earliest and latest channel (XI, XQ, YI, YQ). Includes X/Y and I/Q skew variation.
9. Variation in the skew between X and Y over case temperature, wavelength, input optical power, amplifier gain, and aging. The time for a polarization is defined as the average of I and Q, and the time for an individual I or Q channel is the average of p and n.
10. Variation in the skew between XI and XQ or between YI and YQ over case temperature, wavelength, input optical power, amplifier gain, and aging. The time for an individual I or Q channel is the average of p and n. It is noted that the measurement accuracy of currently available skew measurement techniques may not be sufficient to confirm compliance to limits below 2.0ps.

The TIA differential input current [mA] is calculated as:

$$I_{diff,pp} = 8\sqrt{R_{SIG} \cdot R_{LO} \cdot 10^{(P_{SIG,S}+P_{LO})/10}}$$

where R_{SIG} and R_{LO} are the Signal and LO PD responsivities [A/W], $P_{SIG,S}$ is the Signal power [dBm] in a single polarization (S = X or Y), and P_{LO} is the local oscillator power [dBm]. Assuming a Signal responsivity of 0.10 A/W and an LO responsivity of 0.05 A/W, as well as a 0.80 mA peak to peak differential linear input dynamic range, then a mask for the maximum LO power as a function of Signal power can be calculated as shown in Figure 6-1.



Signal power [dBm]	LO power [dBm]	Diff. input current [mA]
0	3	0.80
-3	6	0.80
-6	9	0.80
-10	13	0.80
-13	16	0.80
-16	16	0.57
-18	16	0.45

Figure 6-1 Informative example: recommended maximum LO power as a function of Signal power for a μICR with R_{SIG} = 0.10 A/W, R_{LO} = 0.05 A/W, and peak-to-peak differential linear input dynamic range of 0.80 mA.

6.2 RF Frequency Response

6.2.1 Measurement Methods

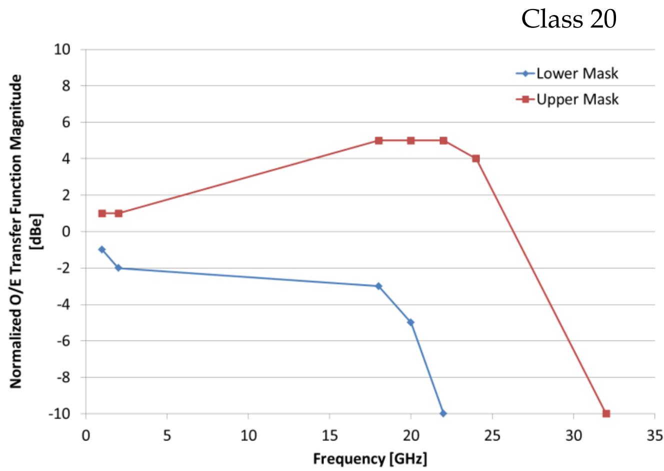
The µICR optical-to-electrical S_{21} transfer function and S_{22} electrical return loss frequency responses shall be measured *differentially* to evaluate conformance to the RF masks in Section 6.2.2 and Section 6.2.3. For these measurements the µICR shall be *soldered* to the measurement test fixture, and the collected data shall be de-embedded to the *RF reference point*. The *RF reference point* is defined as the point on the Host PCB RF traces that is 2.5mm beyond the maximum extent of the µICR RF lead pad (for the Type 1 form factor), or 2.5mm beyond the maximum extent of the solder pad for the RF flexible PCB (for the Type 2 form factor).

The masks below show a *target* range for the optical-to-electrical S_{21} transfer function and S_{22} electrical return loss frequency responses, allowing for component to component variations. These masks may be revised in a future revision of the document as more component and system level performance data becomes available.

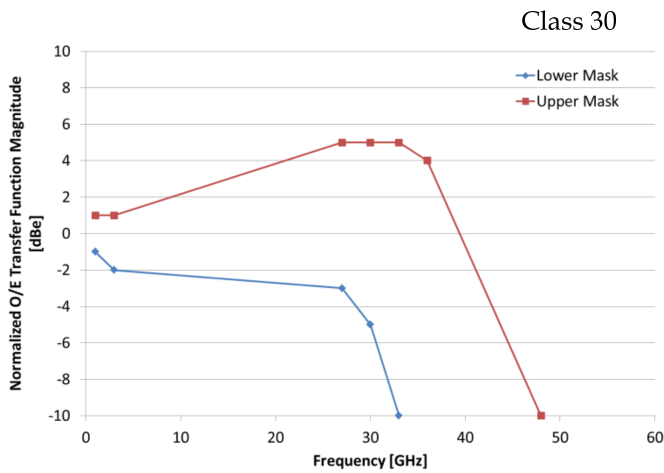
6.2.2 O/E S_{21} Transfer Function Masks

The ideal RF frequency response for the receiver chain of a coherent modem – consisting of the ICR, the differential signal traces between the ICR and the DSP ASIC, and the ADCs at the input of the ASIC – is a low pass response which is flat up to the targeted signal bandwidth and rolls off steeply beyond that. Given that the losses of the signal traces between the ICR and the DSP ASIC increase gradually with frequency, it is generally preferred to have the RF frequency response of the ICR to increase gradually with frequency up to the targeted signal bandwidth, and then roll off steeply.

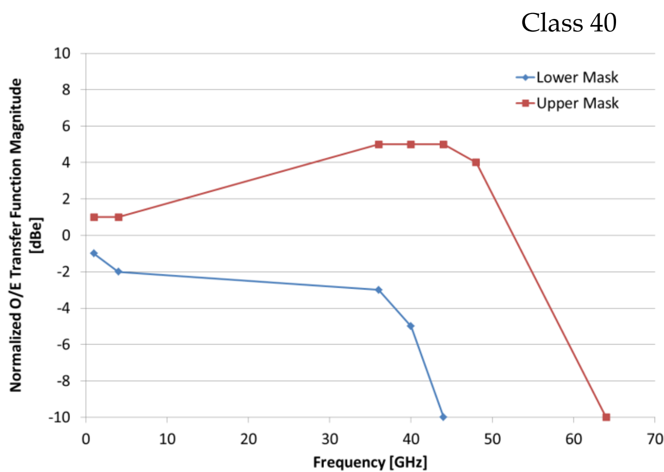
The S_{21} transfer functions shall be measured at a TIA gain condition and µICR temperature that is agreed with the customer. All S_{21} responses shall be normalized to the response at 1GHz. It is assumed that any TIA functionality that manipulates the S_{21} transfer function (i.e. bandwidth adjust functions) can be utilized to obtain compliance with the masks provided in this section.



Frequency [GHz]	Lower Mask [dBe]	Upper Mask [dBe]
1	-1	1
2	-2	1
18	-3	5
20	-5	5
22	-10	5
24		4
32		-10



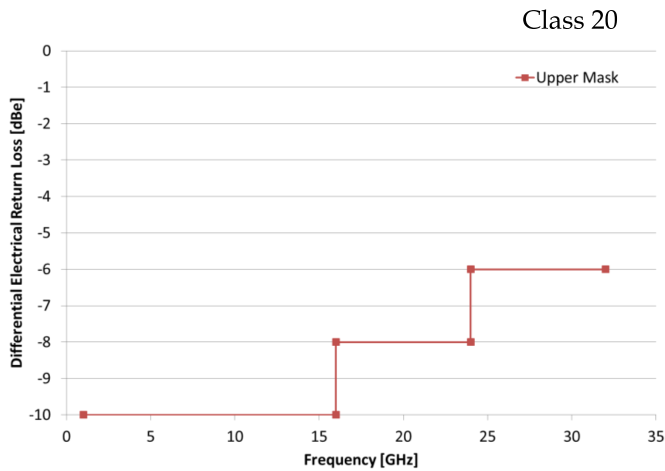
Frequency [GHz]	Lower Mask [dBe]	Upper Mask [dBe]
1	-1	1
3	-2	1
27	-3	5
30	-5	5
33	-10	5
36		4
48		-10



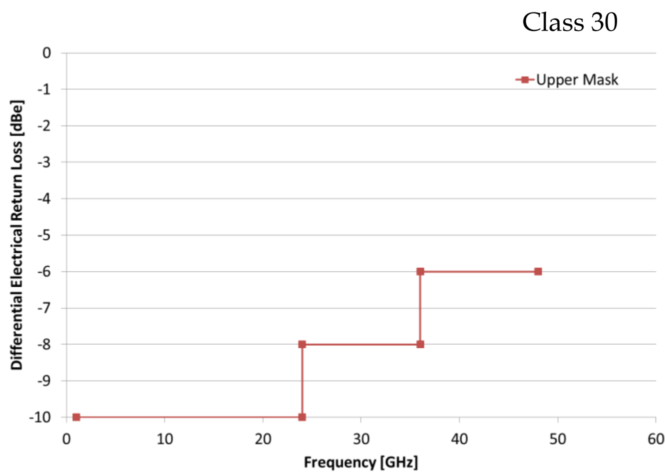
Frequency [GHz]	Lower Mask [dBe]	Upper Mask [dBe]
1	-1	1
4	-2	1
36	-3	5
40	-5	5
44	-10	5
48		4
64		-10

Figure 6-2 Normalized O/E S_{21} transfer function masks for the class 20, 30, and 40 µICR respectively.

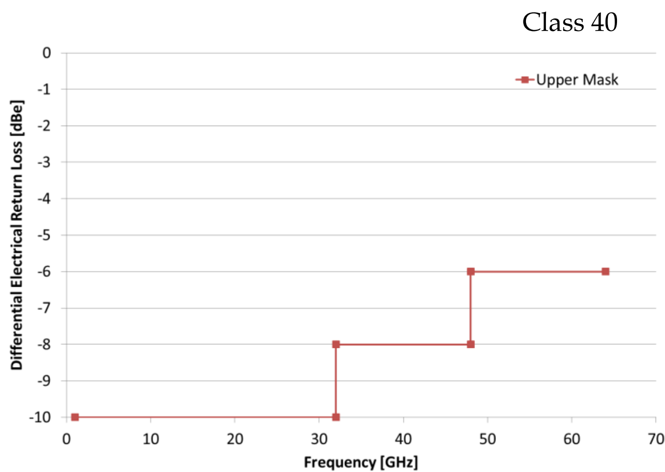
6.2.3 Electrical Return Loss Masks



Frequency [GHz]	Upper Mask [dBe]
1	-10
16	-10
16	-8
24	-8
24	-6
32	-6



Frequency [GHz]	Upper Mask [dBe]
1	-10
24	-10
24	-8
36	-8
36	-6
48	-6



Frequency [GHz]	Upper Mask [dBe]
1	-10
32	-10
32	-8
48	-8
48	-6
64	-6

Figure 6-3 Differential S_{22} electrical return loss masks for the class 20, 30, and 40 µICR, respectively.

7 Mechanical

7.1 General Overview and Fiber Types

Both a primary and alternative electro-mechanical form factor are defined in this revision of the µICR IA. For both form factors the fiber inputs and the RF electrical outputs are located on opposite ends of the package.

The input optical fiber types shall be as defined in Table 7-1.

<table>
<tr><th colspan="2">Parameter</th><th>Unit</th><th>Min</th><th>Typ</th><th>Max</th><th>Note</th></tr>
<tr><td colspan="2">“Minimum bend radius” specification for PMF on Local Oscillator input</td><td>mm</td><td></td><td></td><td>7.5</td><td>1, 2, 3</td></tr>
<tr><td colspan="2">PM fiber bend loss for 10 turns at 7.5mm bend radius</td><td>dB</td><td></td><td></td><td>1</td><td>6</td></tr>
<tr><td rowspan="2">“Minimum bend radius” specification for SMF on Signal input</td><td>Option 1</td><td rowspan="2">mm</td><td></td><td></td><td>5.0</td><td>3, 4</td></tr>
<tr><td>Option 2</td><td></td><td></td><td>7.5</td><td>3, 5</td></tr>
<tr><td colspan="2">SM fiber bend loss for 10 turns at 5.0mm (Option 1) or 7.5mm (Option 2) bend radius</td><td>dB</td><td></td><td></td><td>1</td><td>6</td></tr>
<tr><td colspan="2">Fiber cladding diameter</td><td>µm</td><td></td><td>125</td><td></td><td></td></tr>
<tr><td colspan="2">Fiber coating diameter</td><td>µm</td><td></td><td>250</td><td></td><td></td></tr>
</table>

Table 7-1 Input fiber characteristics.

Notes:

1. The polarization state in the PM fiber shall be aligned to the slow axis of the PM fiber.
2. The slow axis of the PM fiber shall be aligned to the connector key.
3. The PMF color shall be natural (transparent) and the SMF color shall be white (not natural or transparent).
4. The Option 1 SMF shall be compliant to ITU-T Recommendations G.657.B3 and G.652.D.
5. The Option 2 SMF shall be compliant to ITU-T Recommendations G.657.B2 and G.652.D.
6. µICR responsivity shall be measured with straight fibers and shall not include bend loss.

7.2 Type 1 Mechanical Form Factor

The primary electro-mechanical form factor (Type 1) uses a surface mount configuration with the low speed electrical interface signals applied from both the left and right sides of the package. The Type 1 mechanical drawing is shown in Figure 7-1 and the dimensions are provided in Table 7-2. Note that the mounting flanges in Figure 7-1 are optional and un-used DC pins are not required to be present. The Host PCB DC control pin landing pad locations are given in Figure 7-2. Note also the thermal transfer path for a Type 1 µICR shall be from the *Hot-Zone* defined in Figure 7-1 into the Host PCB.

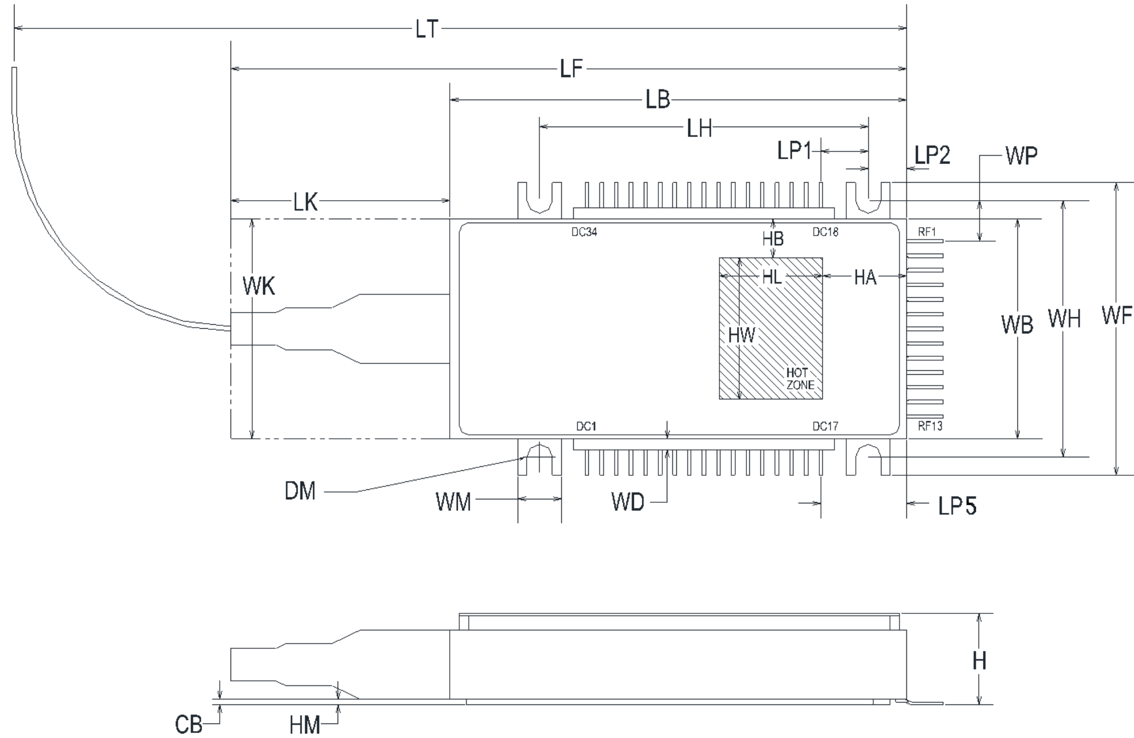


Figure 7-1 Mechanical drawing for Type 1 form factor.

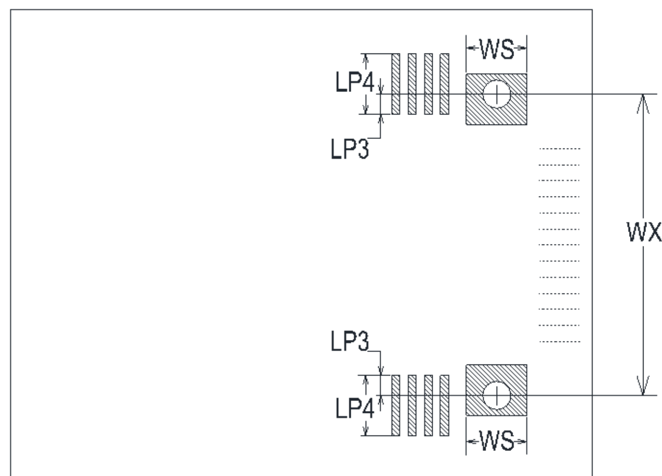


Figure 7-2 Host PCB landing pad locations for low speed pins – Type 1 form factor.

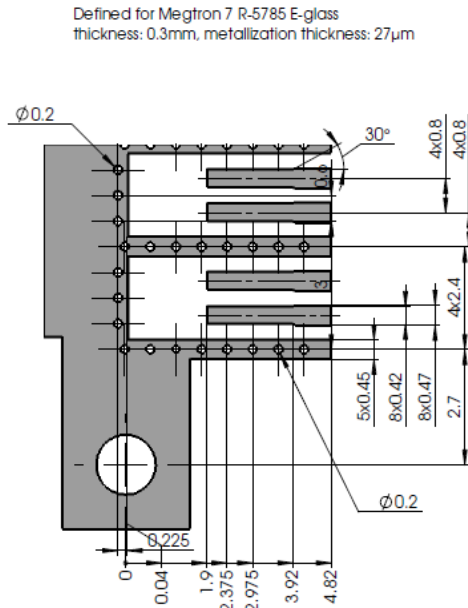


Figure 7-3 Informative host PCB landing pad dimensions for high speed pins – Type 1 form factor.

7.3 Type 2 Mechanical Form Factor

The alternative electro-mechanical form factor (Type 2) employs flexible PCBs for both the RF and single-sided low speed electrical I/O interfaces. The Type 2 mechanical drawing is shown in Figure 7-4 and the dimensions are provided in Table 7-2. The use of flexible PCB in Type 2 allows for a customizable RF connection between a vendor-specific interface on the package and a customer-specific interface on the host PCB. This can provide routing, pitch adjustment and path equalization as needed. One possible adaptation of the low speed and RF interfaces to the CFP2-ACO module environment is illustrated in Figure 7-5 and Figure 7-6, with dimensions related to the mounting given in Table 7-2 and Table 7-3. Note the Type 2 form factor can allow for the direct connection of the µICR *Hot Zone* to the heat sinking surface, for example in the use-case of a pluggable coherent module.

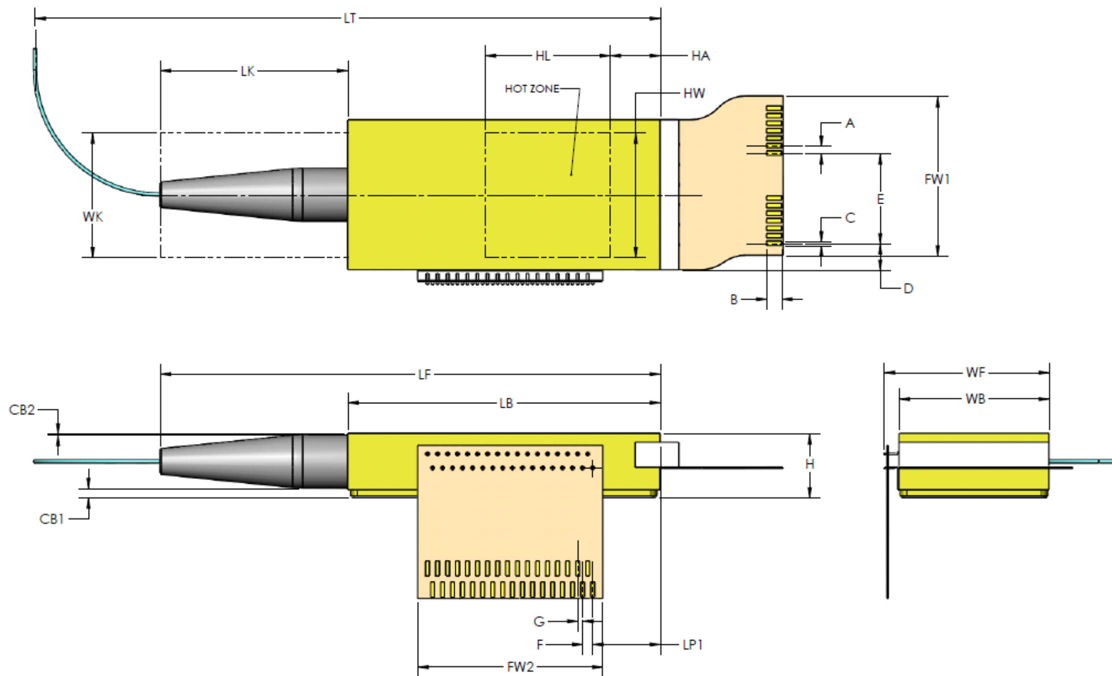


Figure 7-4 Mechanical drawing for Type 2 form factor.

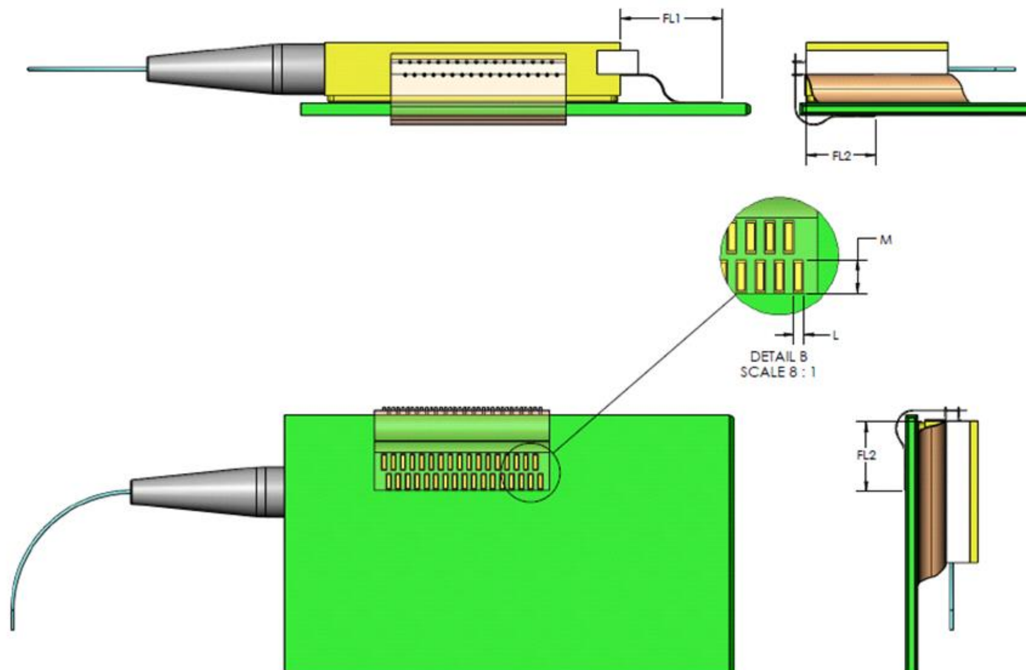


Figure 7-5 Possible adaptation of the Type 2 form factor low speed and RF interfaces to the CFP2-ACO module environment.

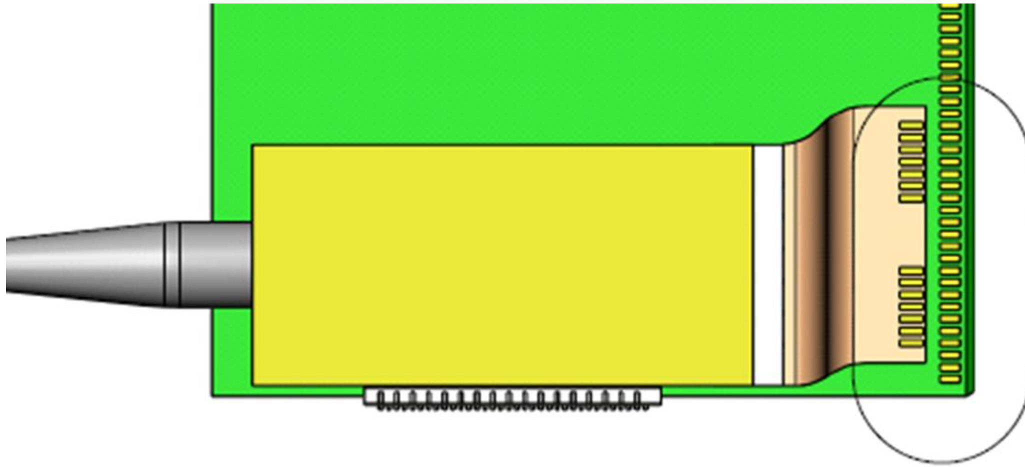


Figure 7-6 Possible adaptation of the Type 2 form factor to the CFP2-ACO module environment – RF interface detail.

7.4 Type 1 and Type 2 Mechanical Form Factor Dimensions

Mechanical dimensions for the Type 1 and Type 2 form factors are combined together in Table 7-2. Table 7-3 provides possible dimensions for the adaptation of the Type 2 form factor low speed and RF interfaces to the CFP2-ACO module environment.

Sym	Description	Type 1 Dimensions			Type 2 Dimensions			Notes
		Min	Nom	Max	Min	Nom	Max	
H	Package height			6.0			6.0	
LT	Total length including 90 degree fiber bends			58			55	
LF	Full length of package including fiber boots			43			40	
LB	Length of package body			27	21		25	
LH	Distance between mounting holes (optional)		18					
LP1	Distance between mounting hole center and center of last DC pin (optional)		2.6			5.4		
LP2	Distance between mounting hole center and RF end of package (optional)		2.1		-	-	-	Type 1
LP3	DC/Control pin PCB landing pad location relative to mounting hole center		1.0		-	-	-	Type 1 Note 2
LP4	DC/Control pin PCB landing pad length		3.0		-	-	-	Type 1
LP5	Distance between center of last DC pin and the RF end of package		4.7					
WF	Width of package including mounting flanges and DC pins			16		13.5		
WH	Distance between mounting foot cutout centers (optional)		14		-	-	-	Type 1
WB	Width of package body		12			12		
WP	Distance between mounting foot cutout center and first RF pin center (optional). RF pins are centered in package.		2.2		-	-	-	Type 1 only
HA	Location of hot region relative to package end	3		5	3		5	
HB	Location of hot region relative to package edge	HW to be centered in package						
HW	Width of hot region			WB			WB	Center

Sym	Description	Type 1 Dimensions			Type 2 Dimensions			Notes
		Min	Nom	Max	Min	Nom	Max	
HL	Length of hot region			10			10	
WK	Width of boot area keep-out region			WB			10	Type 2 Center
LK	Length of boot area keep-out region	(max LF) - LB			(max LF) - LB			Max
WM	Width of mounting flanges (optional)	2	2.4	3	-	-	-	Type 1
HM	Height of mounting flanges (optional)		0.3	0.4	-	-	-	Type 1 Note 1
CB	Clearance under fiber boots	0.25			-	-	-	Type 1
CB1	Clearance between boot and cold side	-	-	-	0.25			Type 2
CB2	Clearance between boot and hot side	-	-	-	0.15			Type 2
DM	Diameter of mounting holes (optional)	1.35	1.4	1.45	-	-	-	
WS	Width of mounting foot PCB pad		3.0					
WD	Edge of DC feed-through ceramics to edge of package frame	0		0.6	-	-	-	
WX	Distance between PCB mounting hole center		15					Type 1

Table 7-2 Type 1 and Type 2 mechanical form factor dimensions (in mm).

Notes:

1. Optional mounting flanges can be either screw-down or solder type.
2. LP3 is offset towards the package body. Refer to Figure 7-2.

Sym	Parameter	Dimension		
		Min	Nom	Max
A	Pad pitch		0.8	
B	Pad length (Contact length between flex pad and PCB pad)	1.0	1.2	1.5
C	Pad width		0.35	
D	Pad offset to package		2.13	
E	Pad offset pitch		7.2	
F	DC Pad pitch		0.8	
FL1	RF flex length formed state		8.6	
FW1	RF flex width on PCB			12.8
G	DC Pad row pitch offset		0.4	
J	PCB Pad width		0.42	
K	PCB Pad length		1.42	
L	PCB DC pad width		0.42	
M	PCB DC pad length		1.40	

Table 7-3 Possible dimensions for the adaptation of the Type 2 form factor low speed and RF interfaces to the CFP2-ACO module environment.

8 Low Speed Electrical Interface Implemented using SPI Control

An alternative implementation for the µICR low speed electrical interface that uses SPI control is detailed herein, including the base required registers and command set. The µICR is defined as the *Client* or *Slave* in the SPI interface with the terms used interchangeably.

8.1 SPI Enabled Low Speed Electrical Interface Pin Assignment

The SPI enabled low speed electrical interface pin assignments are provided in Table 8-1. Pins 1, 2, 33 and 34 enable SPI communications to the µICR. The SPI Reset is present on pin 32, providing synergy with the optional RF output shutdown on pin 32 in the all analog low speed interface given in Table 4-1. RF output shutdown in the SPI enabled interface is implemented by SPI control.

Pin 3 is released for *Future Use* because the MGC/AGC selection is implemented by SPI control. Pins 11, 16, 19 and 24 are also released for *Future Use* because both Gain Adjust in MGC mode and Output Adjust in AGC mode are provided by a single set of reconfigurable Analog Adjust pins (A_i) on pins 12, 23, 15, and 20.

The monitor (M_i) pins 10, 25, 17 and 18 shall at a minimum be capable of monitoring the output peak detect signal and the gain control monitor voltage; however, they may optionally support other vendor-specific analog monitoring functions.

#	Symbol	Description		#	Symbol	Description
1	SPI-MOSI	Master output, Slave (Client) input		34	SPI-CLK	Serial clock
2	SPI-MISO	Master input, Slave (Client) output		33	SPI-CS	Slave (Client) select
3	RFU	Reserved for future use		32	SPI-RST	SPI reset
4	MPD-C	Monitor diode cathode (optional)[3]		31	VOA1	VOA1 Adjust voltage (optional)[2]
5	MPD-A	Monitor diode anode (optional)[3]		30	VOA2	VOA2 Adjust voltage (optional)[2]
6	PD-YI	Photodiode bias voltage YI[1]		29	PD-XQ	Photodiode bias voltage XQ[1]
7	PD-YI	Photodiode bias voltage YI[1]		28	PD-XQ	Photodiode bias voltage XQ[1]
8	PD-YQ	Photodiode bias voltage YQ[1]		27	PD-XI	Photodiode bias voltage XI[1]
9	PD-YQ	Photodiode bias voltage YQ[1]		26	PD-XI	Photodiode bias voltage XI[1]
10	M2	Analogue Monitor YI [Output_PkD or Gain Monitor]		25	M1	Analogue monitor XQ [Output_PkD or Gain Monitor]
11	RFU	Reserved for future use		24	RFU	Reserved for future use
12	A2	Analog output amplitude or gain adjust YI		23	A1	Analog output amplitude or gain adjust XQ
13	VCC-Y	Supply voltage amplifier Y		22	VCC-X	Supply voltage amplifier X
14	GND	Ground Reference		21	GND	Ground Reference
15	A3	Analog output amplitude or gain adjust YQ		20	A0	Analog output amplitude or gain adjust XI
16	RFU	Reserved for future use		19	RFU	Reserved for future use
17	M3	Analogue Monitor YQ [Output_PkD or Gain Monitor]		18	M0	Analogue Monitor XI [Output_PkD or Gain Monitor]

Table 8-1 SPI enabled low speed electrical interface pin assignment.

Notes:

1. PD-YI, PD-YQ, PD-XI, PD-XQ are each assigned two pin where either:
    a. Each one of the two pins independently supplies the bias voltage for one of the two differential photodiodes in the labeled Polarization / Phase channel; or
    b. The first of the two pins (6, 8, 27, 29) is connected to both of the differential photodiodes for the labeled Polarization / Phase channel and the other pin (7, 9, 26, 28) is not connected within the µICR.
2. Pins 31 and 30 (VOA1 and VOA2) shall not be connected internally to ground. If separate VOA functions in the X- and Y-polarization channels are implemented, then the X channel shall be controlled by pin 31 (VOA1) and the Y channel shall be controlled by pin 30 (VOA2); both then being referenced to GND.
3. If independent monitor PDs are provided for the X- and Y-polarizations, the cathode of the X-polarization MPD shall be connected to pin 4 (MPD-C); the anode of the X-polarization MPD shall be connected to pin 5 (MPD-A); the cathode of the Y-polarization MPD shall be connected to pin 4 (MPD-C); and the anode of the Y-polarization MPD shall be connected to GND. Internal circuitry providing equivalent functionality is acceptable.

8.2 Functional Diagram of µICR with SPI Interface

An example schematic functional diagram of a µICR with SPI function is shown in Figure 8-1. The SPI control functions can either be implemented in the TIA or using a separate chip in combination with the TIAs. The output/monitor pin of a given channel is indicated as Mi and the control pin of the same channel is indicated as Ai, where i = 0 to 3 corresponding to XI, XQ, YI and YQ respectively.

The SPI interface allows the configuration of the Analogue Monitoring (M_i) and Analogue Adjust (A_i) pins depending on the desired monitoring / control mode, i.e. AGC or MGC mode in the case of input A_i pin, or at what point in the TIA is to be monitored by addressing the appropriate register as detailed in Section 8.7.

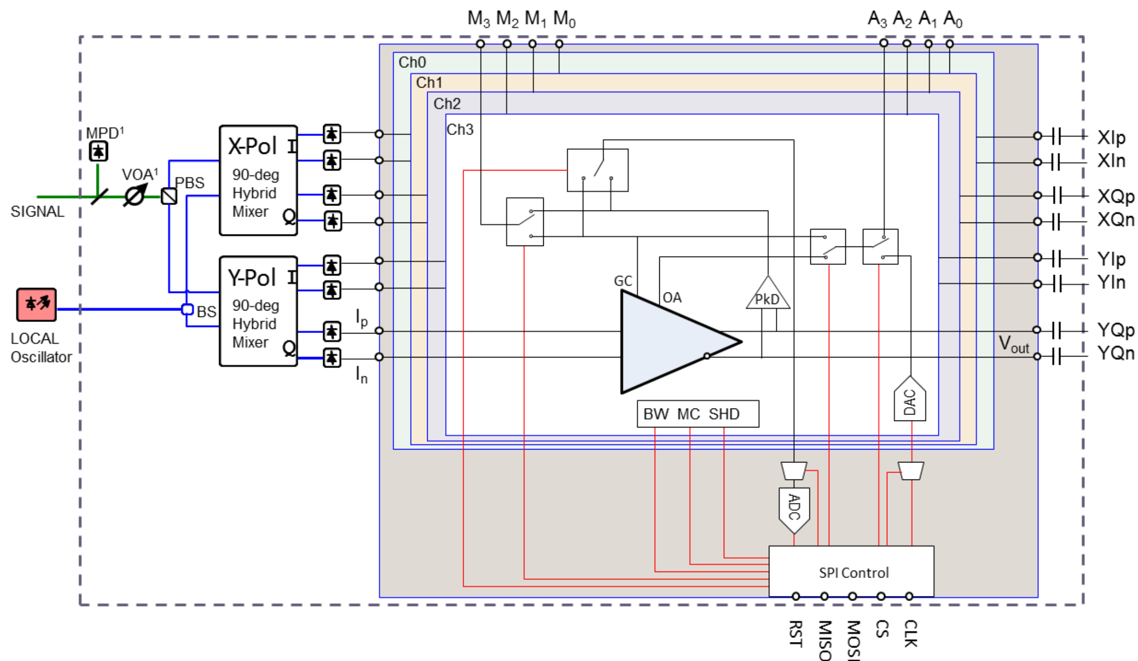


Figure 8-1 Schematic diagram of a µICR with SPI control.

Notes:

1. One configuration for the order of the VOA and MPD is shown. The configuration with the MPD followed by the VOA is an equally acceptable configuration. Configurations having VOA's and/or MPD's after the polarization beam splitter (one VOA/MPD per polarization) are also considered acceptable implementations.
2. The dash-line enclosed area represents the µICR outline.
3. M_i are the analogue monitor pins.
4. A_i are the analogue adjust pins.

8.3 SPI Interface Voltage and Control Specifications

The SPI used is a full duplex high speed synchronous serial interface originally defined by Motorola. The key voltage and control specifications are summarized in Table 8-2.

Parameter	Conditions	Unit	Value	
			min	max
SPI control voltage	Logical 0	V		0.8
	Logical 1		2	
IO Standard	LVCMOS	V	3	3.6
CLK cycle time		ns	50	1000
CLK frequency[1]		MHz	1	20
Time delay between asserting CSN and toggling CLK		ns	25	
Data register width	Address+Op-code	bit	16	
	Data block	bit	16	
Data register shift direction			MSB first	
Clock polarity			Idle state for CLK is low	
Clock phases			Data is latched on the leading edge of CLK, data changes on the trailing edge	
Client select state for data transmission			Chip select low for read/write commands	
Client reset (via Reset pin)			Active low	

Table 8-2 SPI voltage and control specification.

Notes:
1. SPI control can be operated by any specific frequency within the Min/Max range.

8.4 SPI Read / Write Datagram

Below is the data structure of the SPI command datagram.

	Register Address															Op-code	Data Block															
Bit#	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	A 14	A 13	A 12	A 11	A 10	A 9	A 8	A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0	RW	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
Function	reserved						X/ Y	I/ Q	Select register							R W	Data															
value							0/ 1	0/ 1								1 0																

Table 8-3 SPI data telegram structure.

8.5 SPI Read / Write Operation Timing Diagrams

Figure 8-2 and Figure 8-3 detail the SPI write operation timing and the SPI read timing operation.

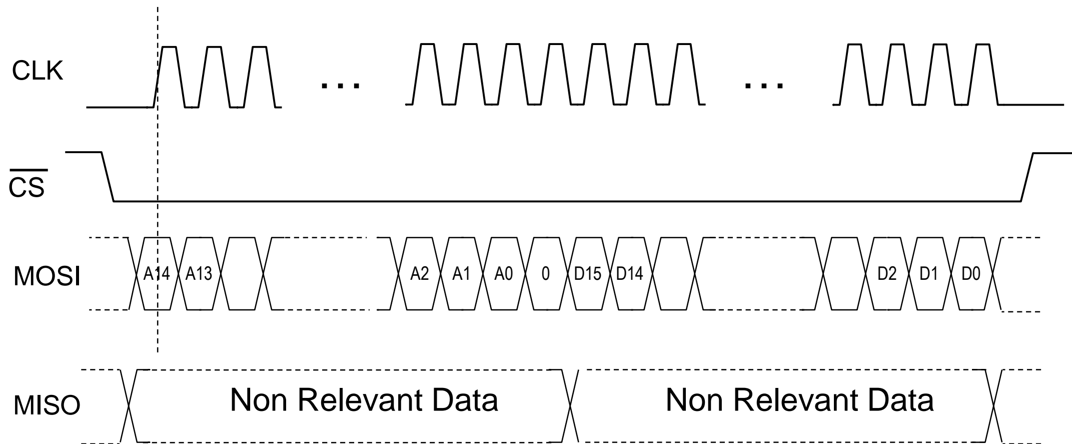


Figure 8-2 SPI write operation timing diagram.

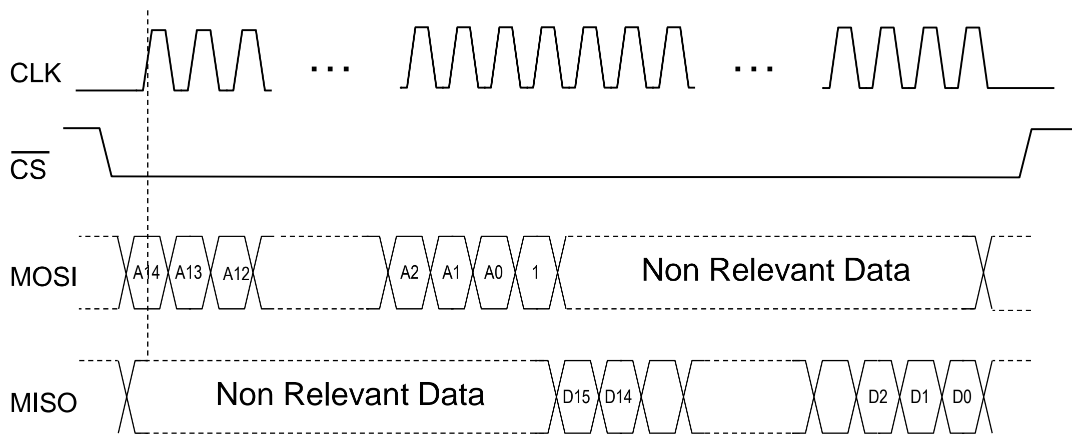


Figure 8-3 SPI read operation timing diagram.

8.6 SPI Timing Specifications

The SPI timing specifications are summarized in Table 8-4 and illustrated in Figure 8-4 and Figure 8-5. The SPI client hardware reset is defined as asynchronous. After the reset, the TIA configuration should be returned to its default, with all outputs shutdown.

Description	Condition	Symbol	Unit	Value	
				min.	max.
CLK clock frequency			MHz	1	20
CLK clock period		t_{CK}	ns	50	1000
CLK peak-peak jitter			ps		500
CLK high time		t_{CKH}	ns	20	550
CLK low time		t_{CKL}	ns	20	550
CLK 10%-90% rise time	15 - 18 pF capacitive load	t_{CKR}	ns	0.5	5
CLK 10%-90% fall time		t_{CKF}	ns	0.5	5
CSN to SPI CLK↑ setup time		t_{CSCK}	ns	50	1000
CLK ↓ to SPI CSN hold time		t_{CKCS}	ns	50	1000
CLK ↓to SPI MISO valid time	15 - 18 pF capacitive load	t_{CKSO}	ns	2	11
MISO 10%-90% rise time	15 - 18 pF capacitive load	t_{SOR}	ns	0.5	5
MISO 10%-90% fall time		t_{SOF}	ns	0.5	5
MOSI to SPI CLK↑ edge setup time		t_{MOCK}	ns	8	
MOSI to SPI CLK↑ edge hold time		t_{CKMO}	ns	8	
MOSI 10%-90% rise time		t_{MOR}	ns	0.5	5
MOSI 10%-90% fall time		t_{MOF}	ns	0.5	5
Min. SPI access inactive time		t_{CSCS}	ns	5*t_{CK}	
RSN time		t_{RS}	ns	t_{CK}	
RSN10%-90% rise time	15 - 18 pF capacitive load	t_{RSR}	ns	0.5	5
RSN10%-90% fall time		t_{RSF}	ns	0.5	5

Table 8-4 SPI read / write timing specifications.

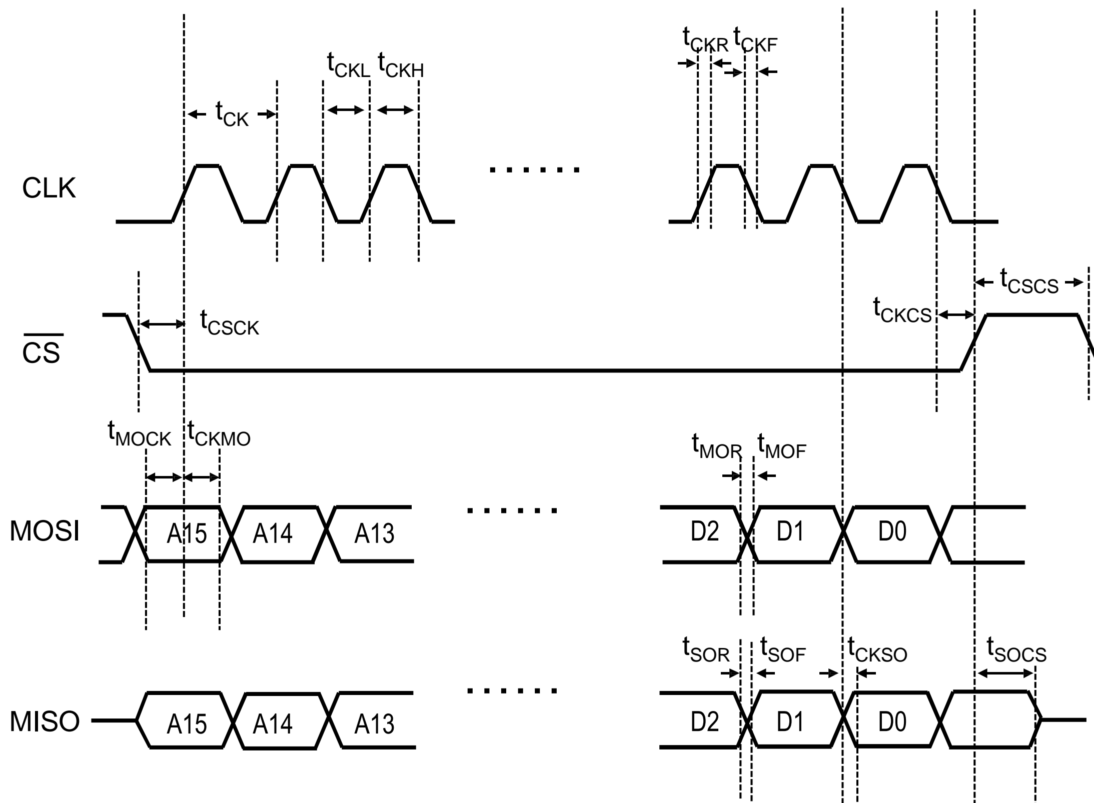


Figure 8-4 SPI client read/write timing.

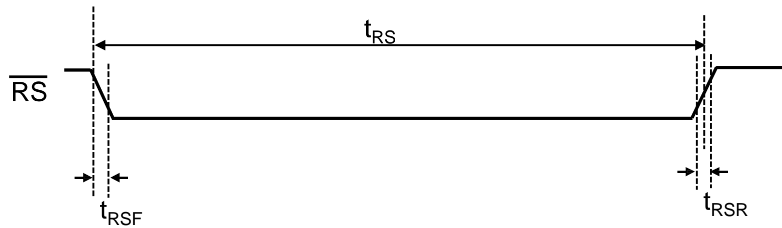


Figure 8-5 SPI client reset timing – asynchronous.

8.7 SPI Registers Specification

For each channel of the device, 32 16-bit registers are designated.

Channel ID	Function	First address	Last address
0	XI	N=0x0000	0x001F
1	XQ	N=0x0080	0x009F
2	YI	N=0x0100	0x011F
3	YQ	N=0x0180	0x019F

Table 8-5 General SPI register mapping.

8.7.1 General Information Registers

General Information Registers are accessible through Channel-0 only. These Registers contain TIA vendor and TIA part ID codes that provide unique identification for a specific SPI function implementation, thus enabling the user to map product specific parameters, performance, register locations, etc., for a given vendor's receiver. These register locations are defined by.

Data	Conditions	Address	<bits>	Default	Access[1]	Type	Notes
TIA vendor ID	Vendor USB code	0x00	<0:15>		Ch0	RO	
RFU	Reserved	0x01	<0:15>		Ch0	RO	
TIA part ID	TIA ID	0x02	<0:15>		Ch0	RO	Vendor defines
RFU	Reserved	0x03	<0:15>		Ch0	RO	
Date or revision		0x04	<0:15>		Ch0	RO	Vendor defines

Table 8-6 General manufacturer information register map.

Notes:

1. Access type = "Ch0" means the register is accessible via channel-0 only, with the same values applicable for all channels.

8.7.2 Base Command Set

The basic functions that are required to be implemented in an SPI controlled µICR are listed in . These base functions are realized by writing / reading data to / from a specific registers as indicated in the table.

Function	Conditions	Address	<bits>	Default	Access[1]	Type	Notes
Reset[2]	Disable	0x05	<0>	0	Ch0	RW	0 = Disable: TIA operational
	Enable						1 = Enable: TIA in reset state
Shutdown[3]	Disable (shutdown disabled)	0x06	<0>	1	Ch0	RW	0 = output active
	Enable (shutdown enabled)						1 = output shutdown
Gain control mode	MGC[4]	0x07	<0>	Vendor specific	Ch0	RW	0 = MGC mode
	AGC[5]						1 = AGC mode
Control mode type	Analogue control via Ai pins	0x07	<1>	0	Ch0	RW	0 = analogue control
	Digital Control via SPI and internal DAC						1 = digital control
Base analogue monitor selection[7]	Output peak detector voltage	N+0x08	<10>	Vendor specific[8]	Channel 0 or Per Channel	RW	1 = selected
	Gain control voltage	N+0x08	<9>	Vendor specific[8]		RW	0 = not selected

Table 8-7 Base set of SPI control functions and registers.

Notes:

1. Access type = "Ch0" means the register is accessible via channel-0 only, with the same values applicable to all channels. "Per channel" means the parameter involved is channel specific.
2. Reset: client soft reset, when enabled it would return all SPI registers to default settings.
3. Shutdown function: When Enabled the RF output is squelched.
4. MGC: manual gain control mode, via setting TIA gain.
5. AGC: automatic gain control mode, via setting TIA output amplitude.
6. Select the analogue monitor parameter for Monitor (Mi) pins. Only one parameter can be selected
7. The vendor specific state for the Analogue Monitor Selection may include a safe "off" state or high impedance state to protect circuitry

8.7.3 Vendor Specific SPI Command Set

Vendor specific SPI functions are listed in . The specific register location for each function is defined by individual vendors.

Function	Conditions	Address	Access[1]	Type	Notes
Analogue monitor selection	Optional: Other monitor signals	N+0x08	Ch0 or Per Channel	RW	<bits> is vendor specific[2] and default is 0
Digital monitor selection [3]	Select monitoring signal for digital readout via SPI	Vendor Specific	Ch0 or Per Channel	RW	
AGC loop BW control	For AGC mode only	Vendor Specific	Ch0 or Per Channel	RW	
TIA BW control		Vendor Specific	Per Channel	RW	
Digital control: OA	Set Output Amplitude via SPI and internal DAC, for AGC mode only	Vendor Specific	Per Channel	RW	
Digital control: GC	Set Gain Control via SPI and internal DAC, MGC mode only	Vendor Specific	Per Channel	RW	
Digital monitor read via SPI	Digital read out of any other parameters as defined by the TIA vendor	Vendor Specific	Per Channel	RO	

Table 8-8 Vendor specific SPI control functions and registers.

Notes:

1. Access type = "Ch0" means the register is accessible via Channel-0 only, with the same values applicable for all channels. . "Per Channel" means the parameter involved is channel specific.
2. Not to conflict with Base Analogue Monitor Selection <bits> in Table 8-7.
3. Examples of parameters for digital monitoring are GC voltage, Output Peak Detector voltage, Input RMS Detector voltage, Input PD current monitor (PDp, PDn), etc.

9 References

9.1 Normative references

9.2 Informative references

- OIF-DPC-RX-01.2 – Implementation Agreement for Integrated Dual Polarization Intradyne Coherent Receivers (November 2013)
- OIF-CFP2-ACO-01.0 – Implementation Agreement for Analogue Coherent Optics Module (January 2016)

10 Appendix A: Glossary

ADC	Analog to Digital Converter
AGC	Automatic Gain Control
BS	Beam Splitter
CMRR	Common Mode Rejection Ratio
DPC	Dual Polarization Coherent [legacy IA name]
DSP	Digital Signal Processor
Gbaud	10^9 Symbols per second
IA	Implementation Agreement
µICR	Micro Intradyne Coherent Receiver
LO	Local Oscillator
MGC	Manual Gain Control
MPD	Monitor Photodiode
MSA	Multi-Source Agreement
OIF	Optical Internetworking Forum
PI	Peak Indicator
PBS	Polarization Beam Splitter
PCB	Printed Circuit Board
PM-QPSK	Polarization Multiplexed Quadrature Phase Shift Keying
SPI	Serial Port Interface
TIA	Trans-Impedance Amplifier
THD	Total Harmonic Distortion
VOA	Variable Optical Attenuator

11 Appendix B: Additional Electro-Optical Characteristics (Informative)

Parameter	Unit	Min	Typ	Max	Note
Gain control bandwidth	MHz		5		1
Total harmonic distortion (THD)	%	For further study			
Signal MPD responsivity	A/W		0.05		2
Signal MPD to LO input optical isolation	dB		45		2
VOA attenuation range	dB	10			2

Table 11-1 Additional electro-optical characteristics (informative).

Notes:

1. Measured by applying step at gain control node such that output changes 5%. BW is estimated by 0.22/Tr where Tr is the 20-80% rise/fall time of the output envelope step.
2. Optional feature.

12 Appendix C: Open issues / current work items

13 Appendix D: List of companies belonging to OIF when document is approved

Acacia Communications
ADVA Optical Networking
Alibaba (China) Co. Ltd.
Amphenol Corp.
Anritsu
Broadcom Limited
Brocade
BRPhotonics
Cavium
China Telecom
Ciena Corporation
Cisco Systems
Coriant
Corning
Credo Semiconductor (HK) LTD
Dell, Inc.
Elenion Technologies, LLC
Fiberhome Technologies Group
Finisar Corporation
Foxconn Interconnect Technology, Ltd.
Fujikura
Fujitsu
Furukawa Electric Japan
Gigamon Inc.
Global Foundries
Google
Hewlett Packard Enterprise (HPE)
Hitachi
Huawei Technologies Co., Ltd.
Infinera
Inphi
Integrated Device Technology
Intel
Invecas
Ixia
Juniper Networks
Kandou Bus
KDDI Research, Inc.
Keysight Technologies, Inc.
Lumentum
MACOM Technology Solutions
Marvell Technology
MaxLinear Inc.
Mellanox Technologies
Microsemi Inc.
Microsoft Corporation
Mitsubishi Electric Corporation
Molex
MoSys, Inc.
MRV
NEC Corporation
NeoPhotonics
Nokia
NTT Corporation
O-Net Communications (HK) Limited
Oclaro
Orange
PETRA
Qorvo
Ranovus
Rianta Solutions, Inc.
Rockley Photonics
Samsung Electronics Co. Ltd.
Samtec Inc.
Semtech
SiFotonics Technologies Co., Ltd.
Silab Tech Private Ltd.
Socionext Inc.
Spirent Communications
Sumitomo Electric Industries
Sumitomo Osaka Cement
TE Connectivity
Tektronix
Teledyne LeCroy
TELUS Communications, Inc.
UNH InterOperability Laboratory (UNH-IOL)
Verizon
Viavi Solutions Deutschland GmbH
Xilinx
Yamaichi Electronics Ltd.
ZTE Corporation