Implementation Agreement for Integrated Dual Polarization Micro-Intradyne Coherent Receivers

IA # OIF-DPC-MRX-01.0

March 31st, 2015

Implementation Agreement created and approved
by the Optical Internetworking Forum
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TITLE: **Implementation Agreement for Micro Intradyne Coherent Receivers**
IA # OIF-DPC-MRX-01.0

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ABSTRACT: Implementation Agreement for a micro intradyne coherent receiver (ICR) suitable for inclusion in a coherent CFP2 module.

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Document Revision History

The following table shows the document revision history.

Document	Date	Revisions/Comments
OIF-DPC-MRX-01.0 Initial release oif2013.271.00	10 October 2013	Initial draft text for discussion leading to baseline text
OIF-DPC-MRX-01.0 Update oif2013.271.01	9 May 2014	Updated draft text for discussion leading to baseline text
OIF-DPC-MRX-01.0 Update oif2014.186.00	21st May 2014	Added package variant type 2 with flexible PCB interface and mounting to hot side to CFP2 case. Removed yellow highlights from version .01
OIF-DPC-MRX-01.0 Update oif2014.186.01	21st May 2014	Added SPI bus information
OIF-DPC-MRX-01.0 Update oif2014.186.02	21st July 2014	Reformatted into new template to fix formatting errors. Section 7 on SPI implementation significantly enlarged
OIF-DPC-MRX-01.0 Update oif2014.186.03	31st July 2014	Modified introduction to mention SPI interface Modified text in sections 3.2 and 4.2. Updated Table 7.1 (Function definitions for pins 10,17,18, 25 & 33) Updated notes to table 7.1 Updated text in section 7.1 Updated figure 71. Updated note 1 to table 7.6 Analogue monitor section added to table 7.7 and updated notes. Deleted “analogue monitor mode selection form table 7.8 and updated notes
OIF-DPC-MRX-01.0 Update oif2014.186.04	31st July 2014	Includes edits during Q3 2014 Technical Meeting in Boston.
OIF-DPC-MRX-01.0 Update oif2014.186.05	31st July 2014	Version approved for first Straw Ballot. Includes final edits from Q3 2014 meeting in Boston.
OIF-DPC-MRX-01.0 Update oif2014.186.06	22nd October 2014	Accept all track changes in oif2014.186.05 Includes comment resolution after first Straw Ballot. Refer to oif2014.314, Comments Resolution Work Sheet. Mounting hole width dimension modified from 14mm to 15mm. See oif2014.311 and oif2014.317. Default state for Analogue Monitor Selection changed to Vendor Specific Table 7-7. Refer to oif 2014.368. (InPhi comment)

OIF-DPC-MRX-01.0 Update oif2014.186.07	20th January 2015	Accept all track changes from oif2014.186.06.. Add two changes to text as agreed at Q4 2014 meeting and shown in oif2014.314.02 which were not shown in oif2015.186.06 by mistake. (Section 1 and section 3.1). Use comments list in oif2015.006 to make the following significant edits Correct Typos. Add superscript reference to Note 8 in the last line of Table7-7 In Table 7-1 SPI-SCLK renamed SPI-CLK. M-XI thru M-YQ named M0 – M3. Also delete note 3&4. In Figure 7-1 re-order M0 thru M3 and A0 thru A3 to agree with table 7-1. Change reset label from RS to RST. Add hyperlinked cross references to Table 10-1 on page 29 and to Figure 10-1, Figure 10-2, and Figure 10-3 in Table 10-1.
OIF-DPC-MRX-01.0Update oif2014.186.08	2nd May 2015	Preparation for Publishing. Accept track changes from oif2014.186.07. Add list of OIF members at this date.

Table 0-1 Document Revision History

1 Introduction

This document details an implementation agreement for an integrated micro intradyne coherent receiver initially targeting coherent CFP2 100G PM-QPSK applications with nominal symbol rates up to 32 GBaud. While specifically addressing 100G PM-QPSK applications, this Implementation Agreement strives to remain modulation format and data rate agnostic whenever practical to maximize applicability to future market requirements. This document is not a multi-source agreement, but is expected to be the foundation of future MSAs.

100G DWDM represents a significant development expense for component and system suppliers. Currently available photonics components addressing the market are discrete and varied. A need for integration has been identified in order to meet cost and size objectives. This implementation agreement aims to reduce risk to component suppliers and users by identifying and specifying common features and properties of the devices that will enable them to broadly meet the needs of this emerging market.

This Implementation Agreement originates from the "100G long-distance DWDM integrated photonics" and "CFP2 coherent optics transceiver module" projects, undertaken in the Physical Link Layer working group. This Implementation Agreement defines: (1) Required functionality. (2) High speed electrical interfaces. (3) Low speed electrical interfaces. (4) Mechanical requirements. (5) Environmental requirements. Also included are informative specifications for (6) opto-electronic interfaces. Two electro-mechanical form factors are defined in this revision of the Implementation Agreement. One is a surface mount configuration similar to the first generation ICR. The second form factor employs a flexible circuit RF interface and allows direct connection of the hot surface of the ICR to the heat sinking face of the CFP2 module if required. Differences between Type 1 and Type 2 form factors will be highlighted where appropriate otherwise common characteristics are required between the two. This Implementation Agreement also defines a low speed electrical interface incorporating an SPI bus for control of the TIAs in the coherent receiver. This is equally applicable to the Type 1 and Type 2 formats. The choice of combination of the package form factor and whether the TIA has an SPI interface will be specific to the application and customer preference.

This Implementation Agreement does not define the type of technology used in photonics sub-components, nor expected optical transmission performance of systems using receivers conforming to this Implementation Agreement. This Implementation Agreement is intentionally structured not to preclude differentiation of product or system performance.

2 Functionality

The required functionality for the micro integrated coherent receiver is shown within the dashed line in Figure 2-1. A single component containing the described functionality is required to meet the objectives of this implementation agreement.

As indicated in Figure 2-1, the coherent receiver requires the following basic functionality:

1. Eight (8) photo-detectors, comprised of 4 sets of balanced detectors
2. Four (4) linear amplifiers with differential AC coupled outputs
3. Two (2) ninety degree hybrid mixers with differential outputs
4. A polarization splitting element, separating the input signal into two orthogonal polarizations, with each polarization delivered to a hybrid mixer
5. A polarization maintaining power splitter or polarization splitting element, splitting the local oscillator power equally to the two hybrid mixers.
6. An optical power tap, and monitor photodiode in the signal input path before the signal polarization splitting element.
7. A variable optical attenuator in the signal input path before the signal polarization splitting element.

At a minimum, the first 5 of the above functions must be contained in a single photonics component to meet the objectives for the micro integrated coherent receiver. Items 6 and 7 may not be fitted in certain applications.

The polarization channels are indicated in Figure 2-1 as 'X-Pol' and 'Y-Pol' and the phase channels for each labeled XI, XQ and YI, YQ respectively. The complementary outputs for each channel are labeled 'p' and 'n'. X and Y indicate a pair of mutually orthogonal polarizations of any orientation. I and Q are mutually orthogonal phase channels in each polarization. I and Q are established relative to the phase of the Local Oscillator where the relationship of the phase of the Signal in the Q channel to the Local Oscillator is either advanced or delayed by nominally 90 degrees as compared to the relationship in the I channel. The relative advance or delay of the Q channel in the Y polarization channel should correspond to that in the X polarization channel. The testing method and nomenclature of Figure 10-3 in section 10 shall be used to establish the relative advance or delay of the Q channel with respect to the I channel. Outputs 'p' and 'n' are the complementary outputs for each polarization-phase channel and are such that the output voltage for 'p' increases as the Signal and

Local Oscillator approach the in-phase condition to form constructive interference, and the output voltage for 'n' decreases under the same conditions.

Additional required functionality for the integrated coherent receiver includes:

- Automatic Gain Control (AGC) and/or Manual Gain Control (MGC)
- User settable output voltage swing
- Independent output swing adjustment for each of the four outputs
- Peak indicators for each output

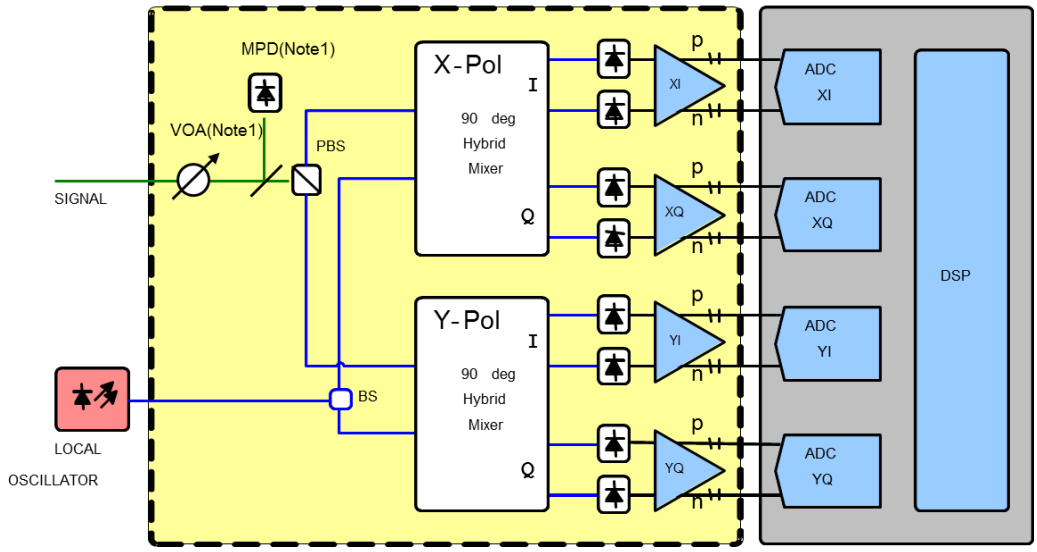


Figure 2-1: Functional diagram of a dual polarization micro intradyne coherent receiver.

Notes:

1. One configuration for the order of the VOA and MPD is shown. The configuration with the MPD followed by the VOA is an equally acceptable configuration.
2. The yellow area enclosed by the dashed line indicates the functionality specified in this implementation agreement.

3 High Speed Electrical Interface

3.1 High Speed Electrical Interface for Type 1

The high speed electrical interface for Type 1 is co-planar waveguide, consistent with the pitch and pin definition detailed in Table 3-1, Table 3-2, and Figure 3-1. It is noted for the channel pin-out shown in Figure 3-1 that X, Y, I, Q, p, and n are consistent with the descriptions in Section 10. It is also noted that alternate polarities for the differential signals specified in Figure 3-1 are acceptable.

Parameter	Value	Notes
Interface Type	Differential	
Channel Number	4	
Channel Configuration	G-S-S-G	Per Figure 3-1
Signal Line Coupling	AC	
Signal Line Impedance	100 ohm Differential	
Channel Pin-Out	XI XQ YI YQ	Per Figure 3-1
Differential Pin-Out	Signal Complimentary Signal	p n

Table 3-1: High-speed electrical interface description

Parameter	Symbol	Min	Typ	Max	Units
Lead Pitch	A		0.8		mm
Lead Length (referenced from outside wall of package, as defined by dimension LP2 in Section 6	B	1.5	2.0	2.5	mm
Signal Lead Width	C	0.1	0.2	0.3	mm
Ground Lead Width	D	0.1	0.2	0.3	mm
Channel Pitch	E		2.4		mm
Signal to Complimentary Signal Pitch	F		0.8		mm

Table 3-2: High-speed electrical interface dimensions

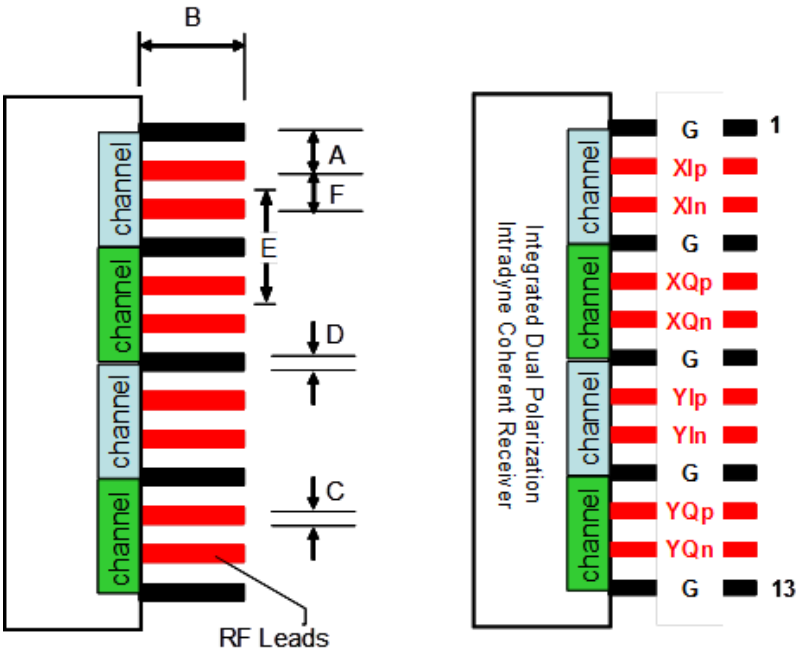


Figure 3-1: High-speed electrical interface definition

3.2 High Speed Electrical Interface Type 2

The high speed electrical interface for the Type 2 form factor is realized using a flexible PCB. This is shown in Figure 3-2. The flexible PCB allows for a customizable RF connection between a vendor-specific interface on the package and a customer-specific interface on the host PCB.

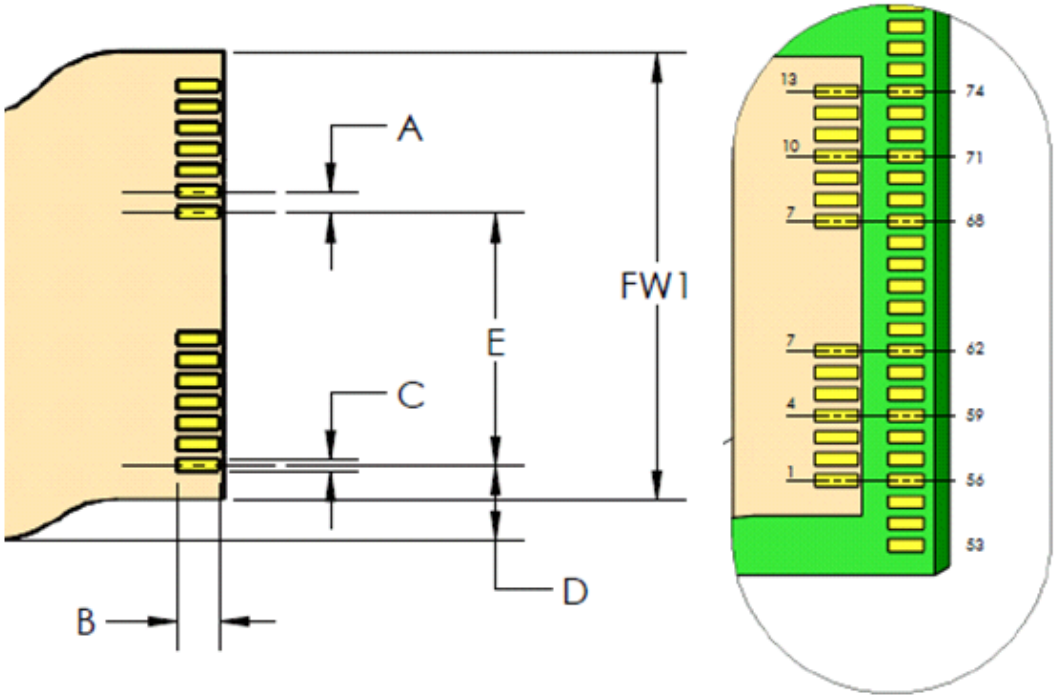


Figure 3-2: High speed flexible PCB interface for Type 2 form factor

In one example, the customer interface of the flexible PCB matches the pitch of a CFP2 connector as shown in Figure 3-2. Numerical values relating to each dimension are given in Table 6-2 and Table 6-3.

4 Low Speed Electrical Interface

4.1 Low Speed Electrical Interface for Type 1

The low speed electrical connections for Type 1 are provided through 34 pins, located on both sides of the package and numbered as shown in Figure 6-1. Any unused pins are not required to be present.

The photocurrent of each photodiode, or a representative equivalent quantity, shall be measurable.

The pin pitch is specified to be 0.8 mm.

The pin definitions for the low speed electrical interface are provided in Table 4-1.

Pin #	Symbol	Description		Pin#	Symbol	Description
1	RFU	Reserved for future use		34	RFU	Reserved for future use
2	RFU	Reserved for future use		33	RFU	Reserved for future use
3	MGC/AGC	MGC/AGC selection (optional)		32	SD	Shutdown (optional)
4	MPD-C	Monitor diode cathode (optional)		31	VOA1	VOA1 Adjust voltage (optional)[2]
5	MPD-A	Monitor diode anode (optional)		30	VOA2	VOA2 Adjust voltage (optional)[2]
6	PD-YI	Photodiode bias voltage YI[1]		29	PD-XQ	Photodiode bias voltage XQ[1]
7	PD-YI	Photodiode bias voltage YI[1]		28	PD-XQ	Photodiode bias voltage XQ[1]
8	PD-YQ	Photodiode bias voltage YQ[1]		27	PD-XI	Photodiode bias voltage XI[1]
9	PD-YQ	Photodiode bias voltage YQI[1]		26	PD-XI	Photodiode bias voltage XI[1]
10	PI-YI	Peak indicator YI		25	PI-XQ	Peak indicator XQ
11	GA-YI	Gain adjust YI		24	GA-XQ	Gain adjust XQ
12	OA-YI	Output amplitude adjust YI		23	OA-XQ	Output amplitude adjust XQ
13	VCC-Y	Supply voltage amplifier Y		22	VCC-X	Supply voltage amplifier X
14	GND	Ground Reference		21	GND	Ground Reference
15	OA-YQ	Output amplitude adjust YQ		20	OA-XI	Output amplitude adjust XI
16	GA-YQ	Gain adjust YQ		19	GA-XI	Gain adjust XI
17	PI-YQ	Peak Indicator YQ		18	PI-XI	Peak Indicator XI

Table 4-1: Low-speed electrical interface definition

Notes

1. PD-YI, PD-YQ, PD-XI, PD-XQ each represent 2 pins wherein each one of the two pins independently supplies the bias voltage to correspondingly each one of the two photodiodes for the labeled Polarization / Phase channel.
2. Pins 31 and 30 (VOA1 and VOA2) shall not be connected internally to ground.

4.2 Low Speed Electrical Interface Type 2

The low speed interface for Type 2 is provided by a 34 pad flexible PCB connected to one side of the package body. The package interface is vendor-specific. The 34 pads on the host PCB are arranged in two rows of 17 pads as illustrated in Figure 4-1. Refer to Figure 6-3 and Figure 6-4. for details.

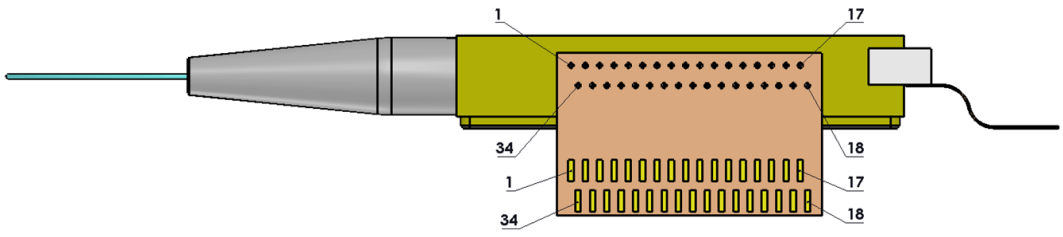


Figure 4-1: Low speed electrical interface Type 2

The pin functions follow those for Type 1 and are shown in Table 4-1.

5 Environmental and Operating Characteristics

Basic operating characteristics are listed in Table 5-1.

Parameter		Unit	Min	Typ	Max	Note
Symbol Rate		G Buad		32		
Operating Frequency	C-band	THz	191.35		196.20	1
	L-band		186.00		191.50	
Amplifier Supply Voltage		V	3.14	3.3	3.47	
Photodiode Bias Voltage	Option 3.3	V	3.135	3.3	3.465	2
	Option 5.0		4.75	5.0	5.25	
Monitor Photodiode Bias Voltage	Option 3.3	V	3.135	3.3	3.465	2
	Option 5.0		4.75	5.0	5.25	
VOA Control Voltage		V	0		9	5
Operating Temperature	Standard	°C	-5		75	3
	Preferred		-5		80	
Operating Humidity		%RH	5		85	4

Table 5-1: Operating characteristics

Notes

1. Minimum supported range. On 50 GHz grid, as defined in G694.1. At least one of the two frequency bands to be supported.
2. Vendor to state which Bias Voltage option or options are allowed both for signal Photodiodes and Monitor Photodiodes.
3. Max temperature is the outside surface temperature of the photonic module and is to be measured in the “hot zone” of the case.
4. Non condensing.
5. Type normally open

6 Mechanical

6.1 General

The mechanical requirements for the micro integrated coherent receiver are detailed in this section. Two mechanical forms are shown. Type 1 is a surface mount format which is similar to the first generation intradyne coherent receivers. See related documents in section 8.2. Type 2 has a flexible PCB RF interface and allows the hot side of the ICR package to be attached to the heat sink face of the CFP2 package if desired.

The requirements include:

- Fiber input and high speed electrical output located on opposite ends of the package
- Signal input fiber to be Single Mode Fiber (SMF)
- Local oscillator fiber to be Polarization Maintaining Single Mode Fiber (PM SMF)
- DC supply and control voltages applied from the left and right sides of the package for Type 1 and from one side only for Type 2. See Figure 6-1 and Figure 6-3
- The thermal transfer path shall be through the PCB side of the device for Type 1

- The devices hot region shall be within the area indicated in Figure 6-1 and Figure 6-3
- Use of appropriate strain relief in high speed electrical pins for Type 1

Parameter		Unit	Min	Typ	Max	Note
Recommended Minimum Fibre Bend radius: PM-SMF on Local Oscillator Input	Standard	mm	20			1,2,3
	Preferred		15			
Recommended Minimum Fibre Bend Radius SMF on Signal Input		mm	15			
Fibre Buffer Diameter		µm		250		

Table 6-1: Fiber characteristics

Notes

1. The polarization state in any PM fiber shall be aligned to the slow axis of the PM fiber.
2. The slow axis of any PM fibers shall be aligned to the connector key.
3. All fibers to be uniquely identified.

6.2 Type 1 Form Factor

Mechanical drawings for Type 1 are shown in the following figures.

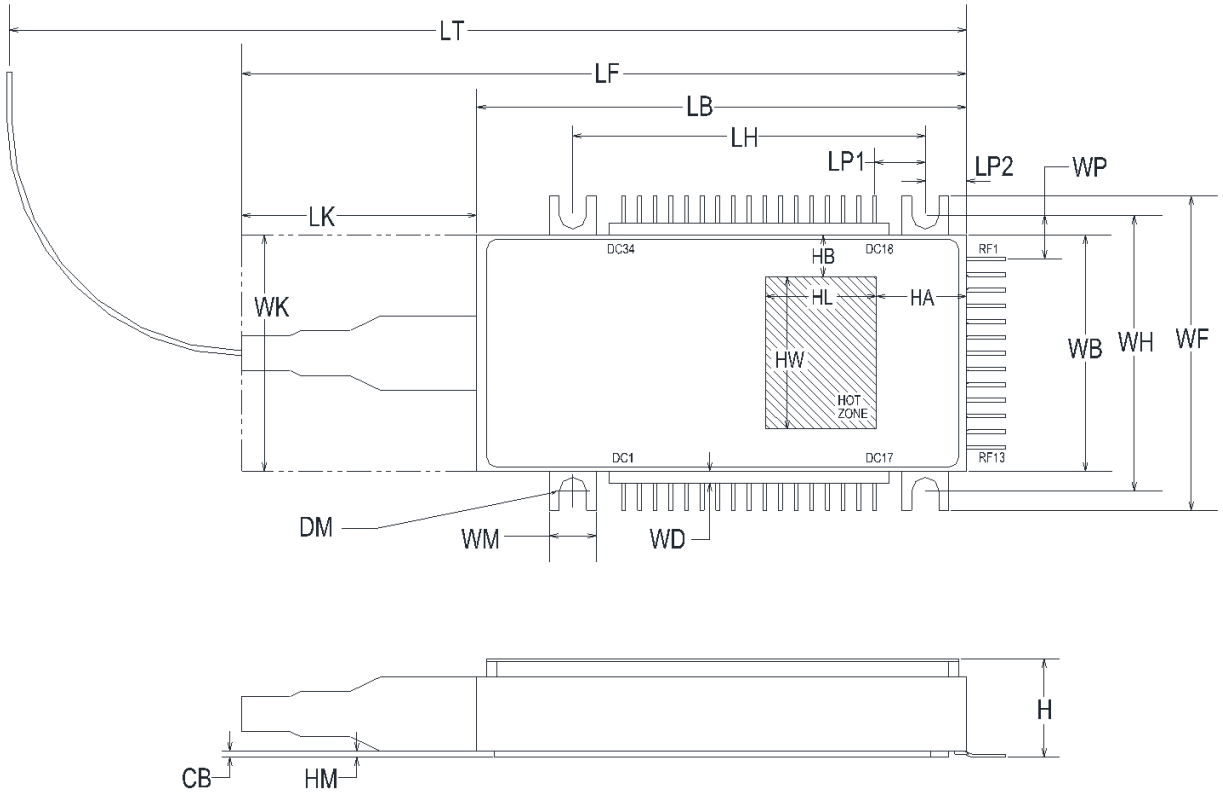


Figure 6-1: Mechanical diagram for Type 1 form factor

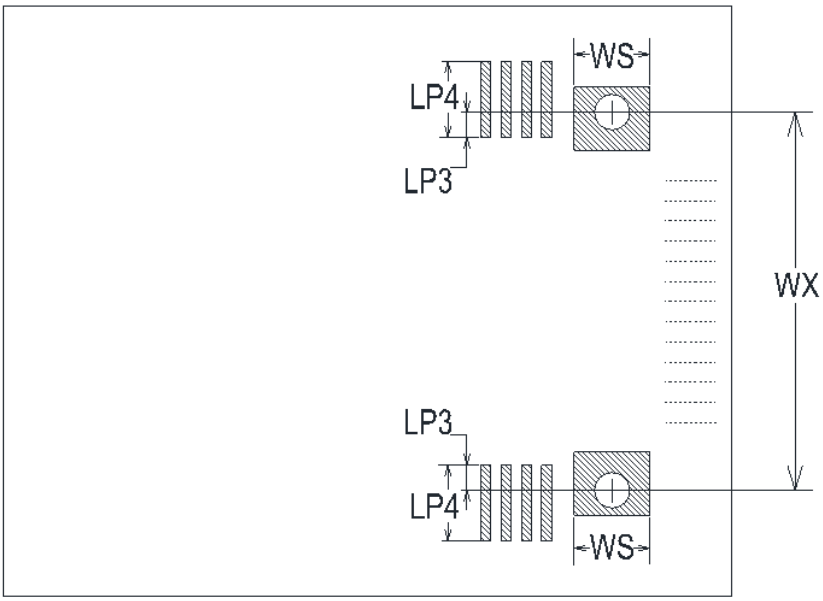


Figure 6-2: Mounting flange and DC/control pin landing pad location

6.3 Type 2 Form Factor

Mechanical drawings for Type 2 are shown in the following figures.

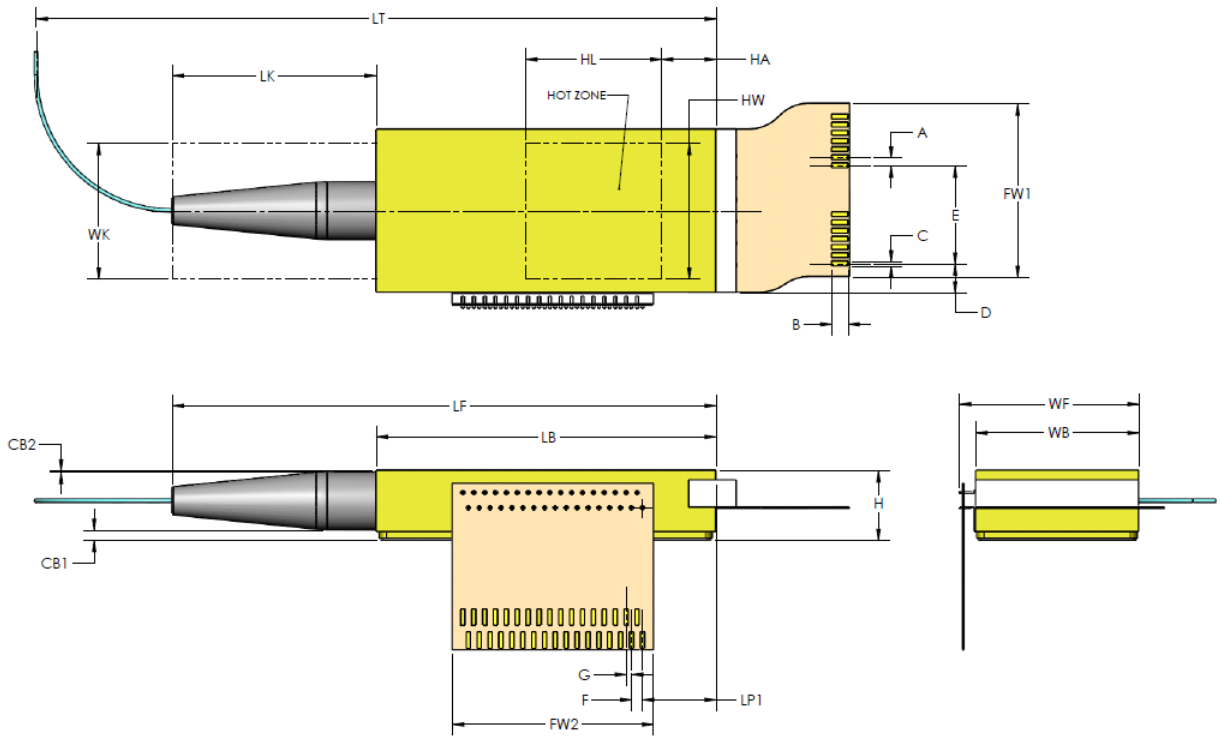


Figure 6-3: Mechanical diagram for Type 2 form factor

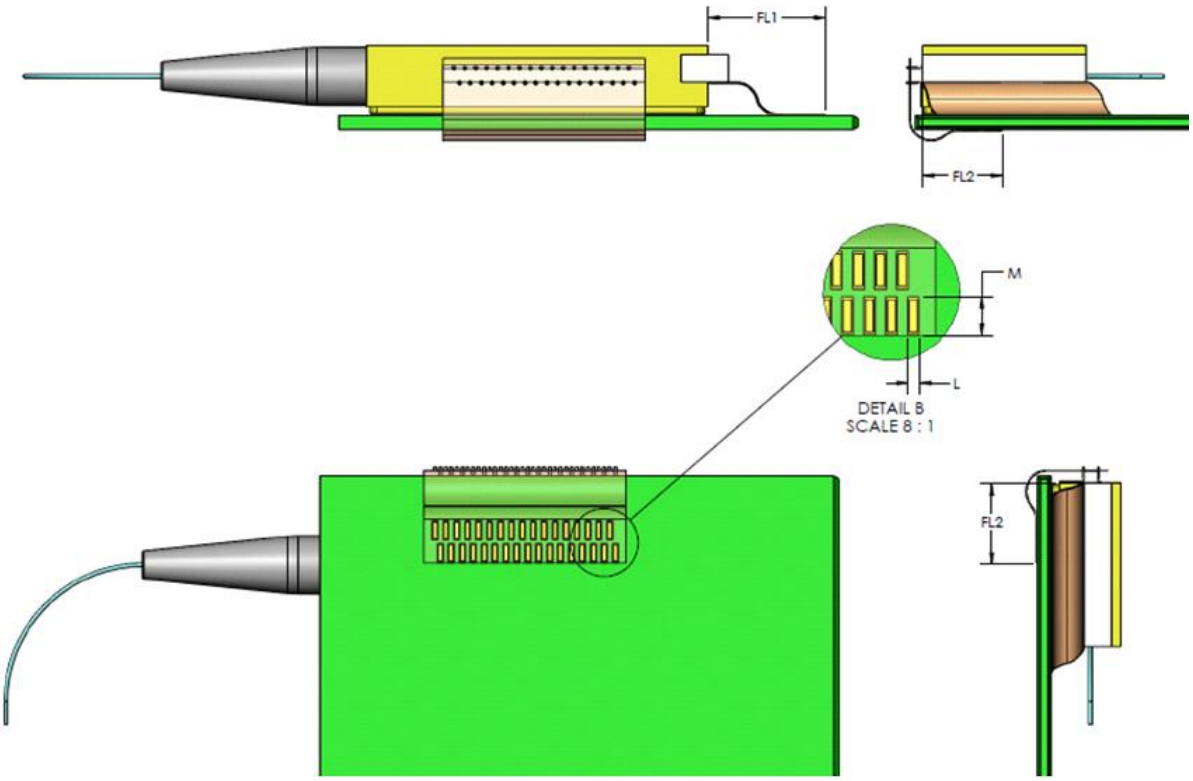


Figure 6-4: A possible mounting method for Type 2 form factor

The flexible PCB allows for a customizable RF connection between a vendor-specific interface on the package and a customer-specific interface on the host PCB, providing routing, pitch adjustment and path equalization as needed. Adaptation to the RF interface of a CFP2 module is illustrated in Figure 6-3 and Figure 6-5 with dimensions as given in Table 6-2 and Table 6-3.

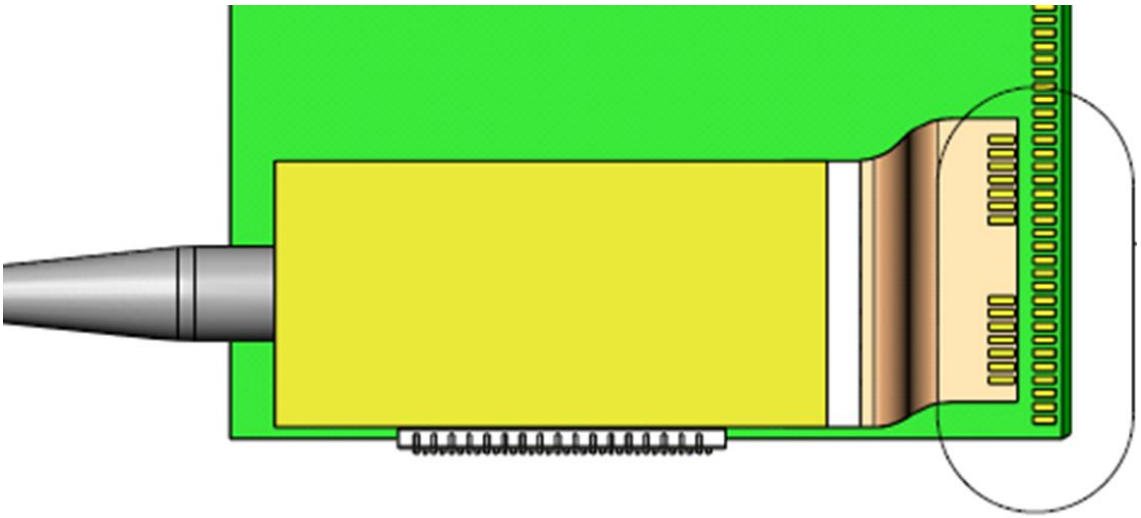


Figure 6-5: Flexible PCB details

6.4 Dimension Table

The dimensions for the two form factors are combined in Table 6-2 and Table 6-3 which follow.

Symbol	Description	Type 1 Dimensions			Type 2 Dimensions			Note
		Min	Nom	Max	Mon	Nom	Max	
H	Package height	3.5		6.0	3.5		6.0	
LT	Total length including 90 degree fiber bends			58			55	
LF	Full length of package including fiber boots			43			40	
LB	Length of package body			27	21		25	
LH	Distance between mounting holes (optional)		18					
LP1	Distance between mounting hole center and center of last DC pin		2.6			5.4		
LP2	Distance between mounting hole center and RF end of package		2.1		-	-	-	Type 1 only
LP3	DC/Control pin landing pad location relative to mounting hole center		1.0		-	-	-	Type 1 only. Note 2
LP4	DC/Control pin landing pad length		3.0		-	-	-	Type 1 only
WF	Width of package including mounting flanges and DC pins			16		13.5		
WH	Distance between mounting foot cutout centres		14		-	-	-	Type 1 only
WB	Width of package body		12			12		
WP	Distance between mounting foot cutout center and first RF pin centre		2.2		-	-	-	Type 1 only
HA	Location of hot region relative to package end	3		5	3		5	
HB	Location of hot region relative to package edge	HW to be centered in package						
HW	Width of hot region			WB			WB	Centered in package
HL	Length of hot region			10			10	
WK	Width of boot area keep-out region			WB			10	Type 2 centered in package
LK	Length of boot area	(max LF)-LB			(max LF)-LB			Maximum

	keep-out region							
WM	Width of mounting flanges	2	2.4	3	-	-	-	Type 1 only
HM	Height of mounting flanges		0.3	0.4	-	-	-	Type 1 only Note 1
CB	Clearance under fibre boots	0.25			-	-	-	Type 1 only
CB1	Clearance between boot and cold side	-	-	-	0.25			Type 2 only
CB2	Clearance between boot and hot side	-	-	-	0.15			Type 2 only
DM	Diameter of mounting holes	1.35	1.4	1.45	-	-	-	
WS	Width of mounting foot pad		3.0					
WD	Edge of DC feed-through ceramics to edge of package frame	0		0.6	-	-	-	
WX	Distance between PCB mounting hole centre		15					Type 1 only

Table 6-2: Mechanical dimensions. (Dimensions in mm)

Notes:

1. Mounting flanges are screw-down and/or solder type.
2. LP3 is offset towards the package body. Refer to Figure 6-3

Dimensions relating to the Type 2 mounting are shown in the following table.

Symbol	Parameter	Dimension			Notes
		Min	Nom	Max	
A	Pad pitch		0.8		Note 1
B	Pad length (Contact length between flex pad and PCB pad)	1.0	1.2	1.5	Note1
C	Pad width		0.35		Note 1
D	Pad offset to package		2.13		Note 1
E	Pad offset pitch		7.2		Note 1
F	DC Pad pitch		0.8		
FL1	RF flex length formed state		8.6		Note 1
FW1	RF flex width on PCB			12.8	Note 1
G	DC Pad row pitch offset		0.4		
J	PCB Pad width		0.42		
K	PCB Pad length		1.42		
L	PCB DC pad width		0.42		
M	PCB DC pad length		1.40		

Table 6-3: Mounting dimensions Type 2 form factor. (Dimensions in mm)

Notes

1. Typical dimension for the illustrative CFP2 RF flex example shown in Figure 6-3, Figure 6-4 and Figure 6-5

7 SPI Interface

The following section defines the implementation of a micro-ICR with SPI control interface for the TIAs along with the base required registers and command set. The micro-ICR is defined as the Client or Slave in the SPI interface. In this section, relating to the SPI specification, the term "Client" and "Slave" are used interchangeably.

7.1 Low-speed Pin Assignment Table

The pin table with SPI control option is shown in Table 7-1

Pin #	Symbol	Description		Pin#	Symbol	Description
1	SPI-MOSI	Master output, slave (client) input		34	SPI-CLK	Serial clock
2	SPI-MISO	Master input, slave (client) output		33	SPI-CS	Client (Slave) select
3	RFU	Reserved for future use		32	SPI-RST	SPI reset
4	MPD-C	Monitor diode cathode (optional)		31	VOA1	VOA1 Adjust voltage (optional)[2]
5	MPD-A	Monitor diode anode (optional)		30	VOA2	VOA2 Adjust voltage (optional)[2]
6	PD-YI	Photodiode bias voltage YI[1]		29	PD-XQ	Photodiode bias voltage XQ[1]
7	PD-YI	Photodiode bias voltage YI[1]		28	PD-XQ	Photodiode bias voltage XQ[1]
8	PD-YQ	Photodiode bias voltage YQ[1]		27	PD-XI	Photodiode bias voltage XI[1]
9	PD-YQ	Photodiode bias voltage YQI[1]		26	PD-XI	Photodiode bias voltage XI[1]
10	M2	Analogue Monitor YI Output_PkD or Gain Monitor		25	M1	Analogue monitor XQ Output_PkD or Gain Monitor
11	RFU	Reserved for future use		24	RFU	Reserved for future use
12	A2	Output amplitude or gain adjust YI		23	A1	Output amplitude or gain adjust XQ
13	VCC-Y	Supply voltage amplifier Y		22	VCC-X	Supply voltage amplifier X
14	GND	Ground Reference		21	GND	Ground Reference
15	A3	Output amplitude or gain adjust YQ		20	A0	Output amplitude or gain adjust XI
16	RFU	Reserved for future use		19	RFU	Reserved for future use
17	M3	Analogue Monitor YQ Output_PkD or Gain Monitor		18	M0	Analogue Monitor XI Output_PkD or Gain Monitor

Table 7-1: Pin table for use with SPI control

Notes

1. PD-YI, PD-YQ, PD-XI, PD-XQ each represent 2 pins wherein each one of the two pins independently supplies the bias voltage to correspondingly each one of the two photodiodes for the labeled polarization / phase channel.
2. Pins 31 and 30 (VOA1 and VOA2) shall not be connected internally to Ground.

Pins 1,2,33 and 34 enable SPI communications to the device. Pin 32 which is the optional output shutdown control in the analogue interface implementation is repurposed as the SPI Reset pin. Output shutdown in the SPI version is implemented by SPI control.

Pin 3 is released for future use because MGC/AGC selection is implemented by SPI control. Pins 11, 16, 19 and 24 are released for future use because both Gain Adjust in MGC mode and Output Adjust in AGC mode are provided by a single set of reconfigurable Analog Adjust pins (Ai).

This monitor pin (Mi) must be capable of monitoring the output peak detect signal and the gain control monitor voltage, but may optionally support other vendor-specific analog monitoring functions.

The adjust pins (Ai) must be capable of supporting the gain control signal in manual gain control mode and the output level adjust setting in automatic gain control mode.

7.2 Functional Diagram of micro-ICR with SPI Interface

An example schematic functional diagram of a micro-ICR with SPI function is shown in Figure 7-1. The SPI control functions can either be implemented in the TIA or using a separate chip in combination with the TIAs. The output/monitor pin of a given channel is indicated as Mi and the control pin of the same channel is indicated as Ai , where i = 0 to 3 corresponding to XI, XQ,YI and YQ respectively. The SPI control allows the configuration of the Analogue Monitoring (Mi) and Analogue Adjusting (Ai) pin depending on the desired monitoring / control mode, i.e. AGC or MGC mode in the case of input Ai pin, or at what point in the TIA is to be monitored by addressing the appropriate register as detailed in section 7.7.

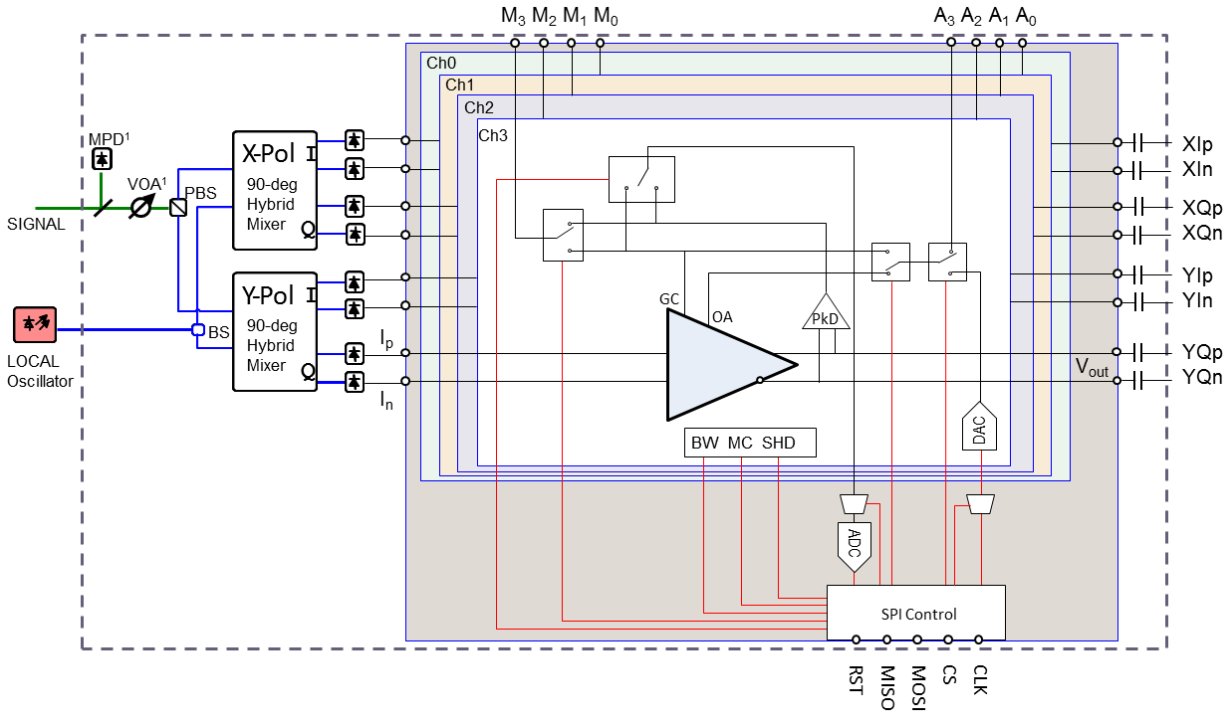


Figure 7-1: Schematic diagram of a micro-ICR with SPI control

Notes:

1. One configuration for the order of the VOA and MPD is shown. The configuration with the VOA followed by the MPD is an equally acceptable configuration
2. The dash-line enclosed area represents the micro-ICR outline.

3. M_i are the analogue monitor pins.
4. A_i are the analogue adjust pins.

7.3 SPI Interface Voltage and Control Specifications

The SPI defined here is a full duplex high speed synchronous serial interface originally defined by Motorola. The key voltage and control specifications are summarized in the Table 7-2 below.

Parameter	Conditions	Value		Unit
		min	max	
SPI control voltage	Logical 0		0.8	V
	Logical 1	2		
IO Standard	LVCMOS	3	3.6	V
CLK cycle time		50	1000	ns
CLK frequency[1]		1	20	MHz
Time delay between asserting CSN and toggling CLK		25		ns
Data register width	Address+Op-code	16		bit
	Data block	16		bit
Data register shift direction		MSB first		
Clock polarity		Idle state for CLK is low		
Clock phases		Data is latched on the leading edge of CLK, data changes on the trailing edge		
Client Select state for data transmission		Chip select low for read/write commands		
Client Reset (via Reset pin)		Active low		

Table 7-2: SPI voltage and control specification

Notes:
1. SPI control can be operated by any specific frequency within the Min/Max range

7.4 SPI Read / Write Datagram

Below is the data structure of the SPI command datagram.

	Register Address															Op-code	Data Block														
Bit#	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	RW	D 15	D 14	D 13	D 12	D 11	D 10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	reserved						X/Y	I/Q	Select register							R	W	Data														
value							0/1	0/1								1	0															

Table 7-3: SPI data telegram structure

7.5 SPI Read / Write Operation Timing Diagrams

Figure 7-2 and Figure 7-3 detail the SPI write operation timing and the SPI read timing operation.

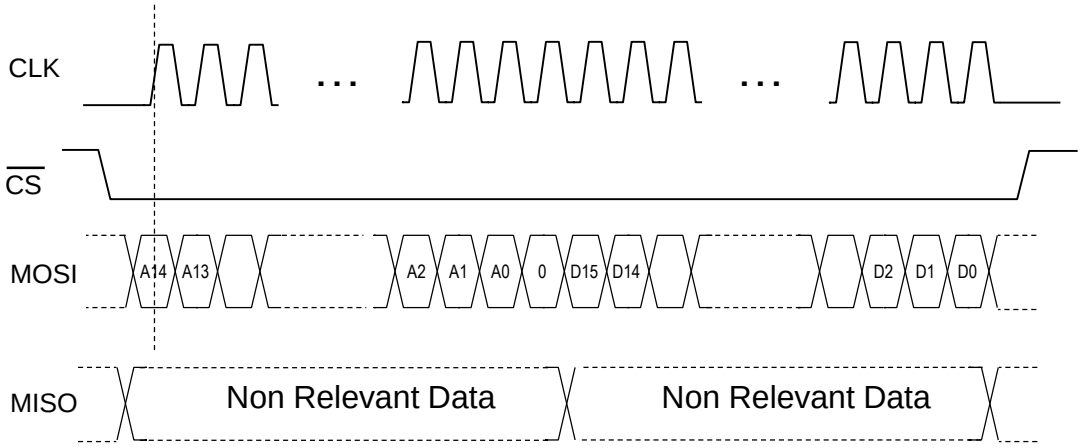


Figure 7-2: SPI write operation timing diagram

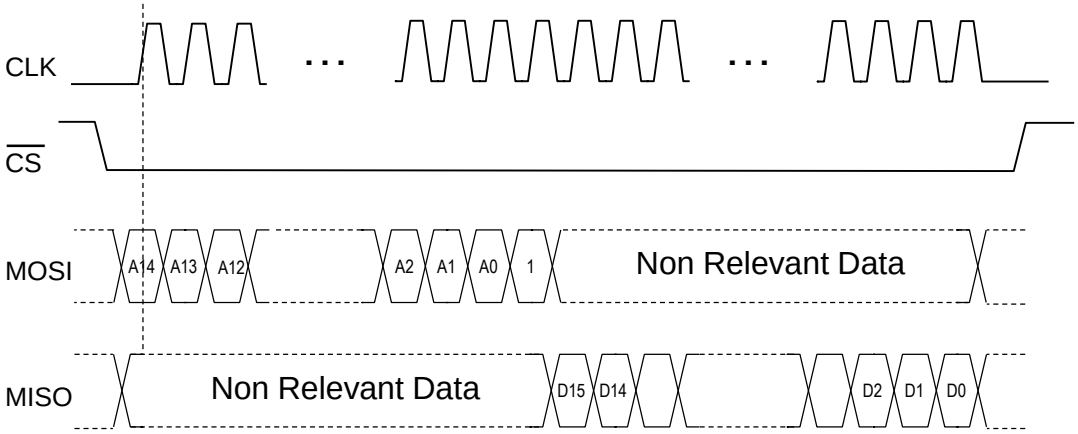


Figure 7-3: SPI read operation timing diagram

7.6 SPI Timing Specifications

The SPI timing specifications are summarized in Table 7-4 below and illustrated in Figure 7-4 and Figure 7-5. The SPI client hardware reset is defined as asynchronous. After the reset, the TIA configuration should be returned to its default, with all outputs shutdown.

Description	Condition	Symbol	Value		Unit
			min.	max.	
CLK clock frequency			1	20	MHz
CLK clock period		t_{CK}	50	1000	ns
CLK peak-peak jitter				500	ps
CLK high time		t_{CKH}	20	550	ns

CLK low time		t_{CKL}	20	550	ns
CLK 10%-90% rise time	15 - 18 pF capacitive load	t_{CKR}	0.5	5	ns
CLK 10%-90% fall time		t_{CKF}	0.5	5	ns
CSN to SPI CLK↑ setup time		t_{CSCK}	50	1000	ns
CLK ↓ to SPI CSN hold time		t_{CKCS}	50	1000	ns
CLK ↓to SPI MISO valid time	15 - 18 pF capacitive load	t_{CKSO}	2	11	ns
MISO 10%-90% rise time	15 - 18 pF capacitive load	t_{SOR}	0.5	5	ns
MISO 10%-90% fall time		t_{SOF}	0.5	5	ns
MOSI to SPI CLK↑ edge setup time		t_{MOCK}	8		ns
MOSI to SPI CLK↑ edge hold time		t_{CKMO}	8		ns
MOSI 10%-90% rise time		t_{MOR}	0.5	5	ns
MOSI 10%-90% fall time		t_{MOF}	0.5	5	ns
min. SPI access inactive time		t_{CSCS}	$5*t_{CK}$		ns
RSN time		t_{RS}	t_{CK}		ns
RSN10%-90% rise time	15 - 18 pF capacitive load	t_{RSR}	0.5	5	ns
RSN10%-90% fall time		t_{RSF}	0.5	5	ns

Table 7-4: SPI read / write timing specifications

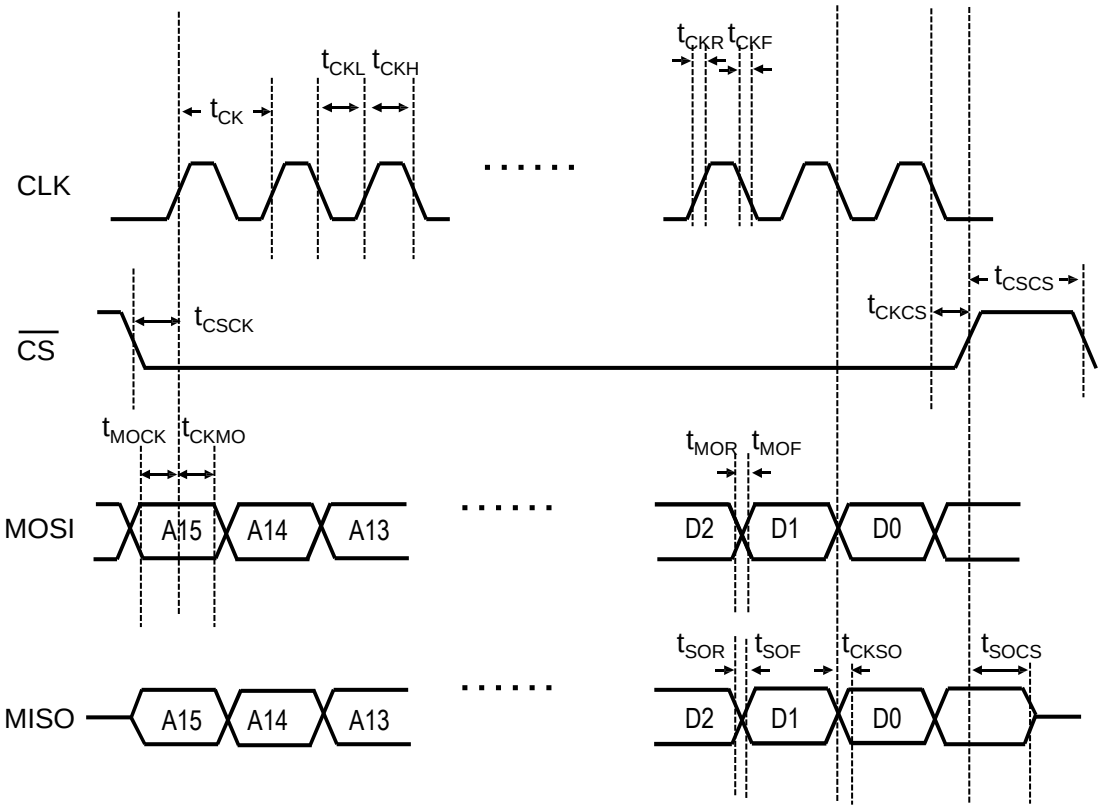


Figure 7-4: SPI client read/write timing

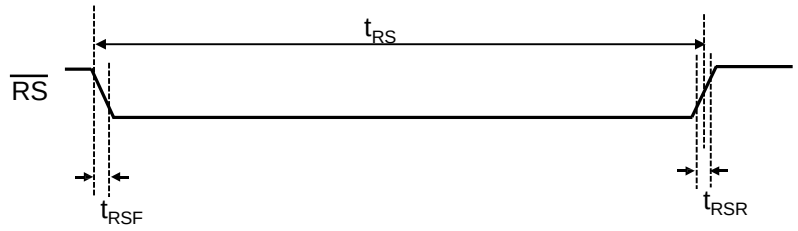


Figure 7-5: SPI client reset timing - asynchronous

7.7 SPI Registers Specification

For each channel of the device, 32 16-bit registers are designated.

Channel ID	function	first address	last address	Notes
0	XI	N=0x0000	0x001f	
1	XQ	N=0x0080	0x009f	
2	YI	N=0x0100	0x011f	
3	YQ	N=0x0180	0x019f	

Table 7-5: General register mapping

7.7.1 General Information Registers

General Information registers are accessible through Channel-0 only. These are Registers containing TIA vendor and TIA part ID codes to provide the unique identification for a specific SPI function implementation to enable the user to map product specific parameters, performance, register locations, etc., for a given vendor's receiver. These register locations are defined by Table 7-6 below.

Data	Conditions	Address	<bits>	Default	Access[1]	Type	Notes
TIA Vendor-ID	Vendor USB code	0x00	<0:15>		Ch0	RO	
RFU	Reserved	0x01	<0:15>		Ch0	RO	
TIA Part-ID	TIA ID	0x02	<0:15>		Ch0	RO	Vendor defines
RFU	Reserved	0x03	<0:15>		Ch0	RO	
Date or Revision		0x04	<0:15>		Ch0	RO	Vendor defines

Table 7-6: General manufacturer information register map

Notes:

1. Access type = "Ch0" means the register is accessible via channel-0 only, with the same values applicable for all channels

7.7.2 Base Command Set

The basic functions that are required to be implemented in an SPI controlled Intradyne Coherent Receiver are listed in Table 7-7. These base functions are

realized by writing / reading data to / from a specific registers as indicated in the table.

Function	Conditions	Address	<bits>	Default	Access[1]	Type	Notes
Reset[2]	Disable Enable	0x05	<0>	0	Ch0	RW	0 = Disable:TIA operational 1 =Enable: TIA in reset state
Shutdown[3]	Disable (shutdown disabled) Enable (shutdown enabled)	0x06	<0>	1	Ch0	RW	0= output active 1 = output shutdown
Gain Control Mode[6]	MGC[4] AGC[5]	0x07	<0>	0	Ch0	RW	0 = MGC mode 1= AGC mode
Control mode type	Analogue control via Ai pins Digital Control via SPI and internal DAC	0x07	<1>	0	Ch0	RW	0 = analogue control 1 = digital control
Base Analogue Monitor Selection[7]	Output peak detector voltage	N+0x08	<10>	Vendor specific[8]	Channel 0 or Per Channel	RW	1=selected 0=not selected
	Gain control voltage	N+0x08	<9>	Vendor specific[8]		RW	

Table 7-7: Base set of SPI control functions and registers

Notes:

1. Access type = “Ch0” means the register is accessible via channel-0 only, with the same values applicable to all channels. “Per channel” means the parameter involved is channel specific.
2. Reset: client soft reset, when enabled it would return all SPI registers to default settings
3. Shutdown function: when enabled it would cause the TIA to squelch RF output
4. MGC: manual gain control mode, via setting TIA gain
5. AGC: automatic gain control mode, via setting TIA output amplitude
6. Default to “1”. i.e AGC mode should also be acceptable
7. Select the analogue monitor parameter for Monitor (Mi) pins. Only one parameter can be selected
8. The vendor specific state for the Analogue Monitor Selection can include a safe "off" state or high impedance state to protect circuitry

7.7.3 Vendor Specific SPI Command Set

Vendor specific SPI functions are listed in Table 7-8. The specific register location for each function may be defined by individual vendors.

Function	Conditions	Address	Access[1]	Type	Notes
Analogue Monitor Selection	Optional: other monitor signals	N+0x08	Ch0 or Per Channel	RW	<bits> is vendor specific[2] and default is 0
Digital Monitor Selection [3]	Select monitoring signal for digital readout via SPI.	Vendor specific	Ch0 or Per channel	RW	
AGC loop BW control	For AGC mode only	Vendor specific	Ch0 or Per channel	RW	

TIA BW control		Vendor specific	Per channel	RW	
Digital Control: OA	Set Output Amplitude via SPI and internal DAC, for AGC mode only	Vendor specific	Per channel	RW	
Digital Control: GC	Set Gain Control via SPI and internal DAC, MGC mode only	Vendor specific	Per channel	RW	
Digital Monitor Read via SPI	Digital read out of any other parameters as defined by the TIA vendor	Vendor specific	Per channel	RO	

Table 7-8: Vendor specific SPI control functions and registers

Notes

1. Access type = “Ch0” means the register is accessible via channel-0 only, with the same values applicable for all channels. . “Per channel” means the parameter involved is channel specific.
2. Not to conflict with Base Analogue Monitor Selection <bits> in Table 7-7
3. Examples of parameters for digital monitoring are GC voltage, Output Peak Detector voltage, Input RMS Detector voltage, Input PD current monitor(PDp, PDn) etc.

8 References

8.1 Normative references

8.2 Informative references

•OIF-DPC-RX-01.2 - Implementation Agreement for Integrated Dual Polarization Intradyne Coherent Receivers (November 2013)

9 Appendix A: Glossary

ADC	Analog to Digital Converter
AGC	Automatic Gain Control
BS	Beam Splitter
CMRR	Common Mode Rejection Ratio
DSP	Digital Signal Processor
GBaud	10^9 Symbols per second
IA	Implementation Agreement
LO	Local Oscillator
MGC	Manual Gain Control
MPD	Monitor Photodiode
MSA	Multi-Source Agreement
OIF	Optical Internetworking Forum
PBS	Polarization Beam Splitter
PCB	Printed Circuit Board
PM-QPSK	Polarization Multiplexed Quadrature Phase Shift Keying

THD Total Harmonic Distortion
VOA Variable Optical Attenuator

10 Appendix B: Opto-Electrical Properties (informative)

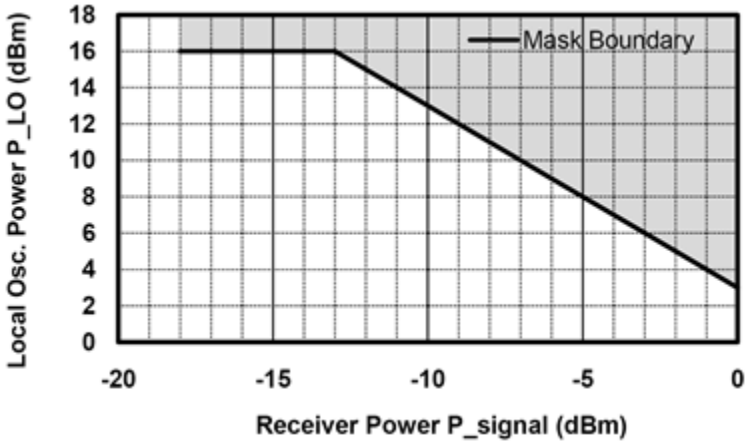
Opto-electrical properties consistent with the application and objectives described in the 100G framework document are provided in Table 10-1. These values are to be interpreted as target values. It is expected that values will be updated as necessary and become normative and moved to the main body of this document as the technology matures.

Parameter	Units	Min	Typ	Max	Comments
Symbol Rate	GBaud		32		
Operating Signal Power	dBm	-18	-10	0	Average optical power
Local Oscillator Power	dBm				See Figure 10-1for recommended operating conditions.
Linear output swing adjustment range Standard Extended	 mVppd mVppd	 300 400	 500	 700 900	Peak to peak, differential, AC coupled
Maximum Gain Control Bandwidth	MHz		5		Settable via external control. Measured by applying step at gain control node such that output changes 5%. BW is estimated by 0.22/Tr where Tr is 20-80% rise/fall of the output envelope step.
Total Harmonic Distortion (THD) DC current = 1.3 mA AC = 0.36mApp in to each PD $V_{OUT\|DIFF}$ = 500mVpp F_{IN} = 1GHz ± 10%	%			5	Assumptions: P(SIG) = -10dBm P(LO) = 13dBm Excess loss = 2dB, PD Responsivity = 0.8A/W
Common Mode Rejection Ratio ($CMRR_{DC}$) Signal to I & Q LO to I & Q	 dBe dBe	 	 	 -20 -12	See Figure 10-2 for definition
Common Mode Rejection Ratio ($CMRR_{22GHz}$) Signal to I & Q LO to I & Q	 dBe dBe	 	 	 -16 -10	See Figure 10-2 for definition
Small Signal Bandwidth (3dB)	GHz		22		
Low Frequency Cutoff	kHz			100	AC coupling

Phase Error	±deg			5	Between XI and XQ and between YI and YQ See Figure 10-3 for test method and nomenclature.
Optical Reflectance	dB			-27	Signal and LO ports. Per ITU-T G.959.1
Output Electrical Return Loss (S22): f < 16 GHz 16 GHz < f < 24 GHz 24 GHz < f < 32 GHz	 dB dB dB	 10 8 6			
Skew: p, n	ps			2	
Channel skew	ps			10	Time difference between earliest and latest channel. Includes channel skew variation.
Channel skew variation	ps			5	Temporal variation in the skew between any 2 channels due to case temperature, wavelength, input optical power, amplifier gain, and aging. Time for channel defined as mean of p and n.
Signal MPD responsivity	A/W		0.05		Optional feature
Signal MPD to LO input optical isolation	dB		45		Optional feature
VOA attenuation range	dB	10			Optional feature

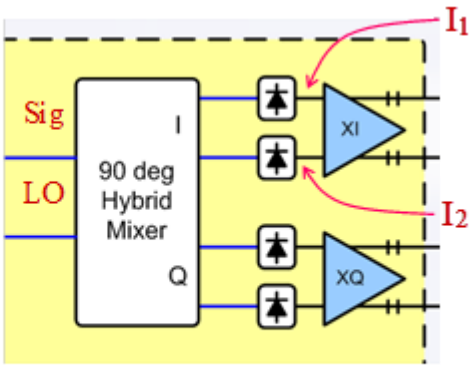
Table 10-1: Opto-electrical properties

Recommended maximum allowable local oscillator power mask as a function of signal power to the integrated receiver for linear operation. A photodiode responsivity of 0.8A/W, NRZ coding, back to back operation, 0.715mA peak to peak differential linear input dynamic range, and an excess loss of 2dB are assumed. P_LO power level is as applied prior to the splitter equally dividing LO between X and Y partitions.



P_signal (dBm)	P_LO (dBm)	I_diff_pp (mA)
0	3	0.715
-3	6	0.715
-6	9	0.715
-10	13	0.715
-13	16	0.715
-16	16	0.506
-18	16	0.402

Figure 10-1: Recommended maximum allowable local oscillator power.



$$CMRR\ (electrical) = 20\log[|I_1 - I_2|/(I_1 + I_2)]$$

Figure 10-2: Definition of CMRR

Test method and nomenclature for the sign of I-Q phase. The measurement shall be made by the heterodyne technique with the frequency of the Signal input greater than the frequency of the LO input and the I and Q channel electrical outputs measured in the time domain. The relative phase shown in (a) shall be referred to as "Advanced-Q" and the relative phase shown in (b) shall be referred to as "Delayed-Q" for the case where 'p' and 'n' RF outputs have the same relative order for both I and Q

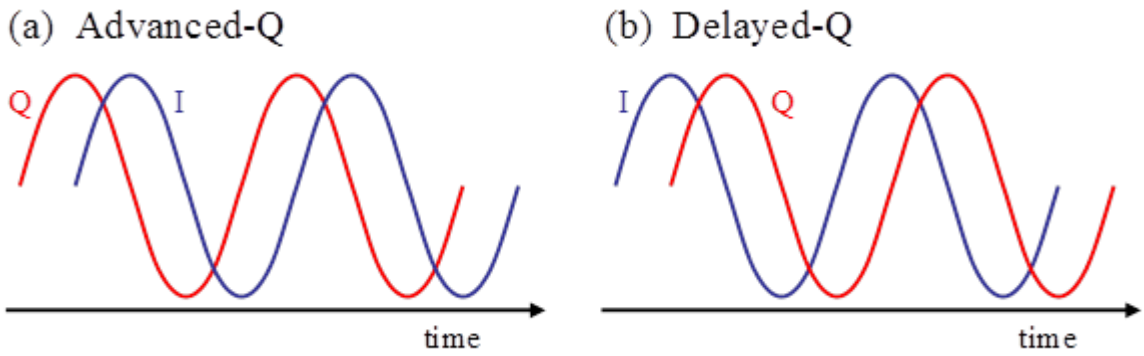


Figure 10-3: Test method and nomenclature for the sign of I-Q phase

11 Appendix B: Open Issues / current work items

12 Appendix C: List of companies belonging to the OIF at approval date

Acacia Communications	Fujikura	NeoPhotonics
ADVA Optical Networking	Fujitsu	NTT Corporation
Alcatel-Lucent	Furukawa Electric Japan	Oclaro
Altera	Google	Orange
AMCC	Hewlett Packard	PacketPhotonics
Amphenol Corp.	Hitachi	PETRA
Analog Devices	Huawei Technologies	Picometrix
Anritsu	IBM Corporation	PMC Sierra
Applied Communication Sciences	Infinera	QLogic Corporation
Avago Technologies Inc.	Inphi	Qorvo
Broadcom	Intel	Ranovus
Brocade	Ixia	Rockley Photonics
BRPhotonics	JDSU	Samtec Inc.
BTI Systems	Juniper Networks	Semtech
China Telecom	Kaiam	Spirent Communications
Ciena Corporation	Kandou	Sumitomo Electric Industries
Cisco Systems	KDDI R&D Laboratories	Sumitomo Osaka Cement
ClariPhy Communications	Keysight Technologies, Inc.	TE Connectivity
Coriant R&G GmbH	LeCroy	Tektronix
CPqD	Luxtera	TELUS Communications, Inc.
Deutsche Telekom	M/A-COM Technology Solutions	TeraXion
Dove Networking Solutions	Mellanox Technologies	Texas Instruments
EMC Corp	Microsemi Inc.	Time Warner Cable
Emcore	Microsoft Corporation	US Conec
Ericsson	Mitsubishi Electric Corporation	Verizon
ETRI	Molex	Xilinx
FCI USA LLC	MoSys, Inc.	Yamaichi Electronics Ltd.
Fiberhome Technologies Group	MultiPhy Ltd	ZTE Corporation
Finisar Corporation	NEC	