Implementation Agreement for CFP2-Digital Coherent Optics Module

IA # OIF-CFP2-DCO-01.0

October 17, 2018

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For additional information contact:
The Optical Internetworking Forum
5177 Brandin Ct, Fremont, CA 94538
510-492-4040 Φ info@oiforum.com

www.oiforum.com

Working Group: **Physical and Link Layer (PLL) Working Group**
Carrier Working Group

TITLE: **Implementation Agreement for CFP2-Digital Coherent Optics Module**
IA OIF-CFP2-DCO-01.0

SOURCE:

TECHNICAL EDITOR

Yida Wen, Ph.D.
Huawei Technologies Co.,Ltd.
Address
Phone: +86 (755)-28972620
Email: wenyida@huawei.com

TECHNICAL EDITOR

Qian Liu
Huawei Technologies Co.,Ltd.
Address
Phone: +86 (27)-59266747
Email: liuqian9@huawei.com

WORKING GROUP CHAIR

David Stauffer, Ph.D.
Kandou Bus
Address
Phone:
Email: david@kandou.com

WORKING GROUP CHAIR

Junjie Li, Ph.D.
China Telecom
Address
Phone: +86 (10)-50902169
Email: lijj.bri@chinatelecom.cn

ABSTRACT: This contribution is the adopted baseline text for the CFP2 Digital Coherent Optics Module Implementation Agreement. OIF2016.297.07 is the original project start document for this project.

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4 Document Revision History

Table 1 provides the OIF-CFP2-DCO-1.0 IA document revision history.

Document	Date	Revisions/Comments
OIF2017.510.00	Oct. 24th 2017	OIF-CFP2-DCO-1.0 DRAFT. Initial Baseline Text Proposal
OIF2017.510.01	Oct. 30th 2017	Modify the REFCLK's minimum input differential voltage and TX/RX MCLK's minimum output differential voltage; Remove the table of part numbers of electrical connectors and reword the description of the section 10.2; Change the client tributary naming of Tx/Rx4 and Tx/Rx6 for the 8x25G mode in the table of pin map;
OIF2017.510.02	Oct. 31st 2017	Minor modifications.
OIF2017.510.03	Nov. 2nd 2017	Modify the Reference 8 and 9; Change the client tributary naming of Tx/Rx4 and Tx/Rx6 for all modes in the Table 6 of pin map in order to fit the Liaison Letter OIF-CFP MSA supporting CFP2-DCO (oif2016.453.00) and the Considerations on CFP2-DCO electrical interface and Pin assignment (oif2017.329.00).
OIF2017.510.04	Jan. 8th 2018	Add the description of optical MUX/De-MUX in section 6; Add the description of pin assignment of two lanes and 6 lanes for 100G and 300G configurations; Modify the Reference 10 and 11.
OIF2017.510.05	Apr. 24th 2018	Add the description of new 25G NRZ electrical lanes and 50G PAM4 electrical lanes in section 5; Add the Reference 13, 14, 15, 16 and 17.
OIF2017.510.06	Apr. 24th 2018	Replace 50GAUI by 50GAUI-1 in section 5; Update the Reference 17.
OIF2017.510.07	July.31st 2018	Update appendix A: Glossary. Revise the description in chapter 5. Add the introduction of high speed management interface in chapter 8.
OIF2017.510.08	Sep. 14th 2018	Update copyright text in Page5. Revise the values in paragraph 9.3.8.

Table 1：IA Document Revision History

5 Introduction

This document details an Implementation Agreement (IA) for a CFP2-DCO Module and defines the CFP2-DCO form factor of an optical transceiver which can support 100Gbit/s, 200Gbit/s, 300Gbit/s and/or 400Gbit/s line interface rates for Ethernet, ITU-T OTN, OIF and other applications. This specification is an extension to the CFP2 MSA MIS v2.6 (r06a) [2] and the CFP2 MSA Hardware Specification Rev. 1.0 [3] to support coherent applications in CFP2 form factor with a digital host interface.

The CFP2-DCO electrical interface will vary by application. The nominal signaling lane rate for applications using 25Gbit/s signaling operates from 25.78-28.20GBd per lane with NRZ modulation as defined in OIF CEI-28G-VSR [6]. When 25 Gbit/s signaling is used for an electrical interface carrying a digital representation of the line interface, the format may use OTL4.4[8] or FOIC1.4[9] formats. When carrying one or more Ethernet clients over the line interface, the electrical interface format may be CAUI-4 [7], 200GAUI-8 [13], 400GAUI-16 [13], 25GAUI [14], LAUI-2 [15], 50GAUI-2 [16], or 100GAUI-4 [16]. The nominal signaling lane rate for applications using 50Gbit/s signaling operates from 25.78-28.20GBd with PAM4 modulation per lane as defined in OIF CEI-56G-VSR PAM4 [11]. When 50 Gbit/s signaling is used for an electrical interface carrying a digital representation of the line interface, the format may use FOIC1.2, FOIC2.4, or FOIC4.8[9] formats. When carrying one or more Ethernet clients over the line interface, the electrical interface format may be 200GAUI-4 [10], 400GAUI-8 [10], 50GAUI-1 [17], or 100GAUI-2 [17].

The CFP2-DCO modules and the host system are hot-pluggable. The module or the host system shall not be damaged by insertion or removal of the module.

This IA specifies key electromechanical aspects of the CFP2-DCO Module that include the following: module mechanical dimensions, electrical connector and pin map, module hardware signaling pins, high-speed electrical characteristics, power supply, power dissipation and management interface.

6 Functional Description

A functional block diagram of the CFP2-DCO is illustrated in Figure 1. Key module functions include transmitter optics, receiver optics, optical MUX/De-MUX in case of multi-carrier link, interface ICs, module controller supporting a MDIO/MDC management interface, and power conversion for a single +3.3V DC power supply from the host. The CFP2-DCO is a hot pluggable module form factor designed for optical networking applications. The module electrical interface has been generically specified to allow for supplier-specific customization around

various 4 × 25Gbit/s interfaces, but can also support potential interfaces such as 8 × 25Gbit/s, 2 × 50Gbit/s, 4 × 50Gbit/s, 6 × 50Gb/s and 8 × 50Gbit/s.

The hot pluggable specifications given in Ref. [3].

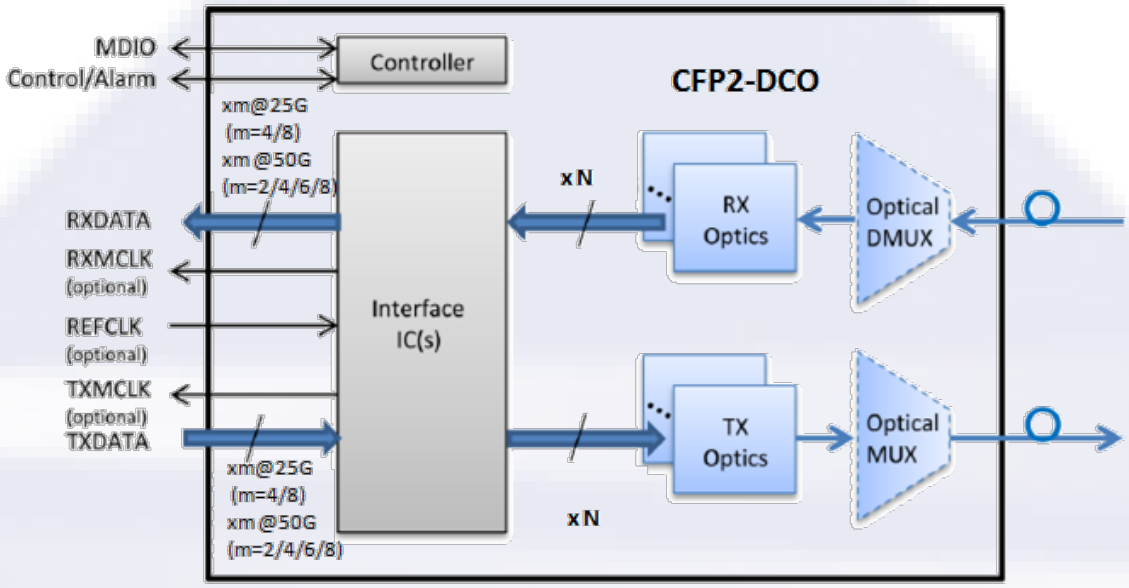

Figure 1: CFP2-DCO Module Basic Functional Block Diagram

7 CFP2-DCO Hardware Signaling Pins

The control and status reporting functions between a host and a CFP2-DCO module use non-data control and status reporting pins on the 104-pin connector. The control and status reporting pins work together with the MDIO interface to form a complete host-CFP2-DCO management interface. The status reporting pins provide status reporting. There are six (6) Hardware Control pins, five (5) Hardware Alarm pins, and five (5) pins dedicated to the MDIO interface. Specification of the CFP2-DCO hardware signaling pins are given in Ref. [3] with the following changes listed in this section.

7.1 Hardware Control Pins

Per specifications given in Ref. [3].

7.2 Hardware Control Pins: Functional Description

Per specifications given in Ref. [3] except for Hardware Interlock as noted below.

7.2.1 Programmable Controls (PRG_CNTLs)

7.2.1.1 Hardware Interlock

The CFP2-DCO module Hardware Interlock function is specified in Ref. [3] with power classes defined in Table 2.

Hardware Interlock Description		Power Class	CFP2-DCO Module Power Dissipation
MSB	LSB		
0	0	1	⩽9W
0	1	2	⩽12W
1	0	3	⩽15W
1	1	⩾4	＞15W

Table 2：CFP2-DCO Module Power Classes defined by Hardware Interlock

7.3 Hardware Alarm Pins

Per specifications given in Ref. [3].

7.4 Hardware Alarm Pins: Functional Description

Per specifications given in Ref. [3].

7.5 Management Interface Pins

Per specifications given in Ref. [3].

7.6 CFP2 Management Interface Hardware Description

Per specifications given in Ref. [3].

7.7 Hardware Signaling Pin Electrical Specifications

Per specifications given in Ref. [3].

7.8 Hardware Signaling Pin Timing Requirements

Per specifications given in Ref. [3].

8 Module Management Interface Description

The CFP2-DCO module utilizes MDIO IEEE Std 802.3™-2015 clause 45 for its management interface. The CFP2-DCO MDIO implementation is defined in a separated document entitled, "CFP MSA Management Interface Specification" [2]. When multiple CFP2-DCO modules are connected via a shared MDIO bus, a particular CFP2-DCO module can be selected by using the Physical Port Address pins.

The higher symbol rates associated with coherent modems points to the utility for a high bandwidth management interface to the modem, for example: accessing the modem overhead data, modem performance monitoring and diagnostic data, and client statistics in contrast to the limited bandwidth access to these facilities possible with the MDIO management interface. This IA allocates additional high-speed signal pins (2-3, 5-6, 47-48, 50-51) to provide an option for such a high-speed interface

9 Performance Specifications

9.1 Operating Environment

Per specifications given in Ref. [3].

9.2 Power Supplies and Power Dissipation

9.2.1 Voltage power supply and power dissipation

The CFP2-DCO module power supply and maximum power dissipation specifications are defined in Table 3.

9.2.2 Inrush current

The inrush current on the 3.3V power supply shall be limited by the CFP2-DCO module to assure a maximum rate of change defined in Table 3.

9.2.3 Turn-off current

The CFP2-DCO module shall limit the turn-off current to assure a maximum rate of change per Table 3.

9.2.4 Power Supply Noise Susceptibility

A host system will supply stable power to the module and guarantee that noise & ripple on the power supply does not exceed that defined in Table 3. A possible example of a power supply filtering circuit that might be used on the host system is a PI C-L-C filter. A module will meet all electrical requirements and remain fully operational in the presence of noise on the 3.3V power supply. The component values of power supply noise filtering circuit, such as the capacitor and inductor, must be selected such that maximum Inrush and Turn-off current does not cause voltage transients which exceed the absolute maximum power supply voltage, all specified in Table 3.

Parameters		Symbol	Min	Typ.	Max	Unit
Absolute Maximum Power supply voltage		VCC	-	-	3.6	V
Total Power Dissipation	Class 1	Pw	-	-	9	W
	Class 2		-	-	12	
	Class 3		-	-	15	
	Class 4		-	-	18	
	Class 5		-	-	21	
	Class 6		-	-	24	
Low Power Mode Dissipation		Plow	-	-	2	W
Operating Power Supply Voltage		VCC	3.2	3.3	3.4	V
Operating Power Supply Current[1]	Class 1 and 2	-	-	-	3.75	A
	Class 3 and 4	-	-	-	5.63	A
	Class 5 and 6	-	-	-	7.5	A
Inrush Current[1]	Class 1 and 2	I-inrush	-	-	200	mA/usec

Turn-off Current		I-turnoff	-200	-	-	mA/usec
Inrush Current[1]	Class 3 and 4	I-inrush	-	-	250	mA/usec
Turn-off Current		I-turnoff	-250	-	-	mA/usec
Inrush Current[1]	Class 5 and 6	I-inrush	-	-	300	mA/usec
Turn-off Current		I-turnoff	-300	-	-	mA/usec
Power Supply Noise		Vrip	-	-	2% 3%	DC-1MHz 1-10MHz

Table 3：Voltage power supply

[1] Maximum current per pin shall not exceed 1000mA. Those power classes for which the maximum current per pin exceeds 1000mA will require agreement from an electrical connecter supplier.

9.2.5 Grounding

Per specifications given in Ref. [3].

9.3 High Speed Electrical Characteristics

The CFP2-DCO Module high speed electrical interface supports the following configurations:

1) 4 Tx lanes + 4 Rx lanes, each at 25Gbit/s (25.78-28.20GBd PAM2);
2) 8 Tx lanes + 8 Rx lanes, each at 25Gbit/s (25.78-28.20GBd PAM2).

Following electrical interfaces may be supported in future:

3) 2 Tx lanes + 2 Rx lanes, each at 50Gbit/s (25.78-28.20GBd PAM4);
4) 4 Tx lanes + 4 Rx lanes, each at 50Gbit/s (25.78-28.20GBd PAM4);
5) 6 Tx lanes + 6 Rx lanes, each at 50Gbit/s (25.78-28.20GBd PAM4);
6) 8 Tx lanes + 8 Rx lanes, each at 50Gbit/s (25.78-28.20GBd PAM4).

Specification of the CFP2-DCO high speed electrical characteristics are given in Ref. [3] with the following changes listed in this section.

The high speed electrical interface shall be AC-coupled within the CFP2-DCO module as is shown in Figure 2.

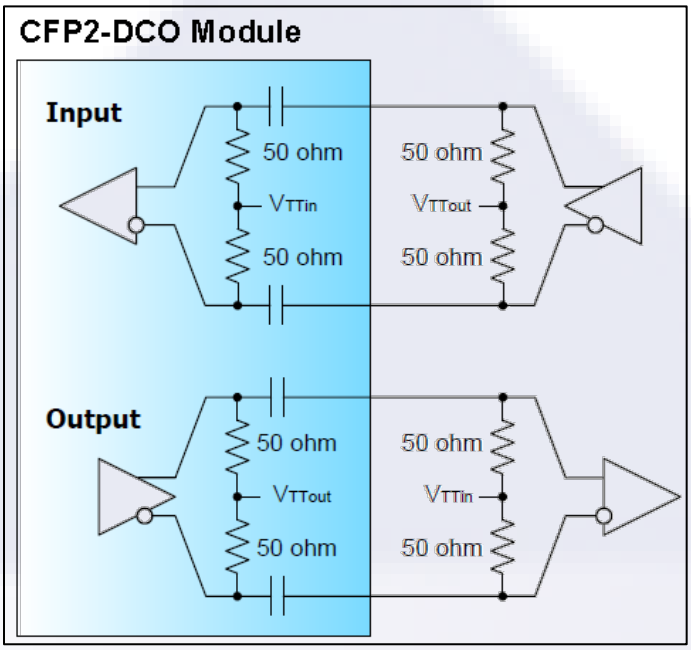

Figure 2: High Speed I/O for Data and Clocks

9.3.1 25Gbit/s Transmitter Data (and Clock)

The 25Gbit/s Transmitter Data is defined in OIF CEI-28G-VSR [6]. Lane orientation and designation is specified in the pin-map tables given in Section 11.7.

9.3.2 25Gbit/s Receiver Data (and Clock)

The 25Gbit/s Receiver Data is defined in OIF CEI-28G-VSR [6]. Lane orientation and designation is specified in the pin-map tables given in Section 11.7.

9.3.3 50Gbit/s Transmitter Data (and Clock)

The 50Gbit/s Transmitter Data is defined in OIF CEI-56G-VSR-PAM4 [11]. Lane orientation and designation is specified in the pin-map tables given in Section 11.7.

9.3.4 50Gbit/s Receiver Data (and Clock)

The 50Gbit/s Receiver Data is defined in CEI-56G-VSR-PAM4 [11]. Lane orientation and designation is specified in the pin-map tables given in Section 11.7.

9.3.5 Loopback (Optional)

The CFP2-DCO module may optionally support loopback functionality. The capability to support the loopback functionality is dependent upon the interface IC technology, labeled as "Interface IC(s)" in the Figure 3. Recommended loopback orientation implementation is Tx0 to Rx0. The host loopback and the network loopback are oriented per Figure 3shown below. The CFP2-DCO module vendor will specify which loopback functionality, if any, is supported. For details on controlling the loopback mode, please refer to Reference [3]. In optional loopback, Txn is looped back to Rxn, for example Tx0+ to Rx0+, on both host and network side.

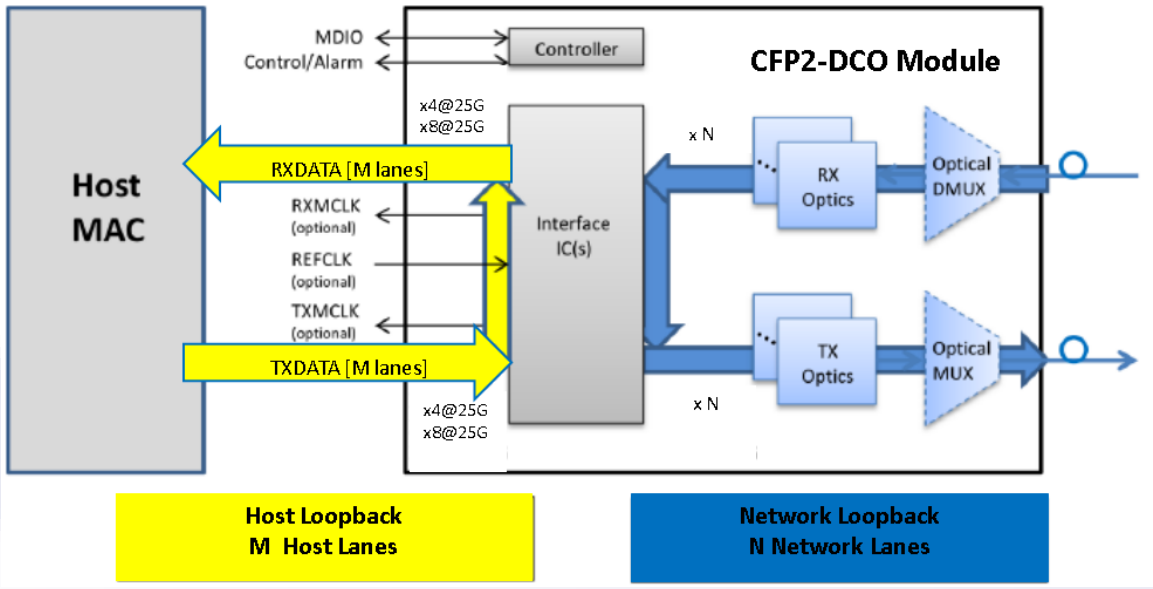

Figure 3: CFP2 Module Optional Loopback Orientation

9.3.6 Reference Clock (Optional)

The host shall optionally supply a reference clock (REFCLK) at 1/160 electrical lane rate for M × 25Gbit/s applications. The CFP2 module may optionally use the 1/40 reference clock for transmitter path retiming, for example for Telecom applications.

When provided, the REFCLK shall be CML differential AC-coupled and terminated within the CFP2-DCO module as shown in Figure 3. There is no required phase relationship between the data lanes and the reference clock, but the clock frequency shall not deviate more than specified in Table 4. For detailed clock characteristics please refer to the below table.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Impedance	Zd	80	100	120	Ω	
Frequency	f		1/160			Of electrical lane baudrate
			1/40			Of electrical lane baudrate
			156.25MHz			for the Ethernet applications
Frequency Stability	Δf	-100		100	ppm	For Ethernet applications
		-20		20		For Telecom applications
Input Differential Voltage	V_{DIFF}	400	500	1200	mV	Peak to Peak Differential
RMS Jitter[2,3]	σ			0.7	ps	Random Jitter.

						Over frequency band of 10kHz < f <20MHz
Clock Duty Cycle		45		55	%	
Clock Rise/Fall Time 10/90%[4]	$t_{r/f}$	200		1250	ps	1/160 of electrical lane rate for M x 25Gbit/s
		50		315		1/40 of electrical lane rate for M x 25Gbit/s

Table 4：Optional Reference Clock Characteristics

[2] The spectrum of the jitter within this frequency band is undefined. The CFP2-DCO shall meet performance requirements with worst case condition of a single jitter tone of 0.7ps RMS at any frequency between 10 kHz and 20MHz. 0.7ps is based on some vendors' experience.

[3] For Telecom applications better frequency may be required.

[4] As per CFP2 MSA recommendation.

9.3.7 Transmitter Monitor Clock (Optional)

The CFP2-DCO optionally may supply a transmitter monitor clock (TXMCLK). This clock is intended to be used as a reference for measurements of the module optical transmit signal. If provided, the clock shall operate at 1/8 of the transmitter optical symbol rate. This rate is optimized for triggering high-speed sampling scopes. Clock termination is shown in Figure 3. TXMCLK characteristics are summarized in Table 5.

9.3.8 Receiver Monitor Clock (Optional)

The CFP2-DCO optionally may supply a receiver monitor clock (RXMCLK). This clock is intended to be used as a reference for measurements of the module receive data. If provided, the clock shall operate at 1/40 of the receiver electrical lane data rate. The RXMCLK may optionally operate at 1/160 of the receiver electrical lane data rate. Clock termination is shown in Figure 3. RXMCLK characteristics are summarized in Table 5.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Impedance	Zd	80	100	120	Ω	
Frequency-TX_MCLK			1/8			Of TX optical symbol rate -default
			1/32			Of TX optical symbol rate - optional
Frequency-RX_MCLK			1/40			Of RX electrical lane data rate - default
			1/160			Of RX electrical lane data rate - optional
Output Differential Voltage	V_{DIFF}	400	500	1200	mV	Peak to Peak Differential
Clock Duty Cycle		45		55	%	

Table 5：CFP2-DCO Module Clocking Signals

10 Mechanical Specifications

10.1 Mechanical Overview

Per specifications given in Ref. [3] and normative engineering drawings of the CFP2 form factor, cages and connectors are given in Ref. [12].

10.2 Electrical Connector

CFP2-DCO's connector to support class 6 (24W) operation must have minimum sustain current-handling of 1A per contact. Classic CFP2 connectors and ports may not support 1A operation, it is outside of this IA to define operation of CFP2-DCO into legacy CFP2 ports.

10.3 CFP2-DCO Module Dimensions

Per specifications given in Ref. [3].

10.4 Host System Dimensions

Per specifications given in Ref. [3].

10.5 Riding Heat Sink

The actual dimensions of the heat sink and cage top opening shall be optimized for the particular host system.

10.6 Optical Connectors

The CFP2 module shall support LC optical connector type. The position of the optical connector in the Y and Z axes shall be specified by the CFP2-DCO module manufacturer. The optical port connections on the front of the CFP2 are detailed in Ref. [3] and Ref. [12]. In addition to the centered duplex LC connector location specified by the CFP MSA, the CFP2-DCO IA also optionally allows the optical port position on the front of the module to be either left or right-justified if needed to enable a certain vendor-specific implementation technology.

10.7 Pin Assignment

The CFP2-DCO connector has 104 pins which are arranged in Top and Bottom rows. The CFP2-DCO connector supports the following configurations:

a) Two (2) 50Gbit/s TX lanes plus two 50Gbit/s RX lanes;
b) Four (4) 25Gbit/s or 50Gbit/s TX lanes plus four 25Gbit/s or 50Gbit/s RX lanes;
c) Six (6) 50Gbit/s TX lanes plus six 50Gbit/s RX lanes;
d) Eight (8) 25Gbit/s or 50Gbit/s TX lanes plus eight 25Gbit/s or 50Gbit/s RX lanes.

The CFP2-DCO connector top row and bottom row pin assignments for the N×25Gbit/s and 50Gbit/s configurations are illustrated in Table 6. Detailed description of the bottom row pins 1 through pin 52 are given in Table 7. Note the REFCLK pins are located on the top row along with the high-speed TX and RX

data pins. A single-ended REFCLK is an option. The CFP2-DCO connector pin map orientation is shown in Figure 4.

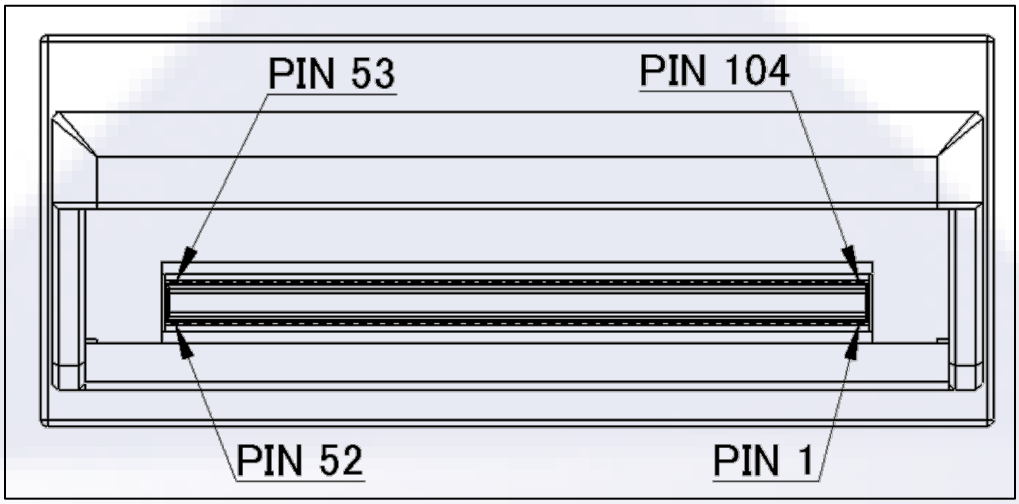

Figure 4: CFP2-DCO Connector Pin Map Orientation

Pin view from top ==> Host

	Bottom
1	GND
2	*(TX_MCLKn) or Vendor_Out0n*
3	*(TX_MCLKp) or Vendor_Out0p*
4	GND
5	Vendor_In0n
6	Vendor_In0p
7	3.3V_GND
8	3.3V_GND
9	3.3V
10	3.3V
11	3.3V
12	3.3V
13	3.3V_GND
14	3.3V_GND
15	VND_IO_A
16	VND_IO_B
17	PRG_CNTL1
18	PRG_CNTL2
19	PRG_CNTL3
20	PRG_ALRM1
21	PRG_ALRM2
22	PRG_ALRM3
23	GND
24	TX_DIS
25	RX_LOS
26	MOD_LOPWR
27	MOD_ABS
28	MOD_RSTn
29	GLB_ALRMn
30	GND
31	MDC
32	MDIO
33	PRTADR0
34	PRTADR1
35	PRTADR2
36	VND_IO_C

	Top (4x25G)
104	GND
103	N.C.
102	N.C.
101	GND
100	TX3n
99	TX3p
98	GND
97	TX2n
96	TX2p
95	GND
94	N.C.
93	N.C.
92	GND
91	N.C.
90	N.C.
89	GND
88	TX1n
87	TX1p
86	GND
85	TX0n
84	TX0p
83	GND
82	N.C.
81	N.C.
80	GND
79	*(REFCLKn)*
78	*(REFCLKp)*
77	GND
76	N.C.
75	N.C.
74	GND
73	RX3n
72	RX3p
71	GND
70	RX2n
69	RX2p

	Top (8x25G)
104	GND
103	TX4n
102	TX4p
101	GND
100	TX3n
99	TX3p
98	GND
97	TX2n
96	TX2p
95	GND
94	TX5n
93	TX5p
92	GND
91	TX6n
90	TX6p
89	GND
88	TX1n
87	TX1p
86	GND
85	TX0n
84	TX0p
83	GND
82	TX7n
81	TX7p
80	GND
79	*(REFCLKn)*
78	*(REFCLKp)*
77	GND
76	RX4n
75	RX4p
74	GND
73	RX3n
72	RX3p
71	GND
70	RX2n
69	RX2p

37	VND_IO_D
38	VND_IO_E
39	3.3V_GND
40	3.3V_GND
41	3.3V
42	3.3V
43	3.3V
44	3.3V
45	3.3V_GND
46	3.3V_GND
47	Vendor_In1n
48	Vendor_In1p
49	GND
50	*(RX_MCLKn) or Vendor_Out1n*
51	*(RX_MCLKp) or Vendor_Out1p*
52	GND

68	GND
67	N.C.
66	N.C.
65	GND
64	N.C.
63	N.C.
62	GND
61	RX1n
60	RX1p
59	GND
58	RX0n
57	RX0p
56	GND
55	N.C.
54	N.C.
53	GND

68	GND
67	RX5n
66	RX5p
65	GND
64	RX6n
63	RX6p
62	GND
61	RX1n
60	RX1p
59	GND
58	RX0n
57	RX0p
56	GND
55	RX7n
54	RX7p
53	GND

	Top (2x50G)
104	GND
103	N.C.
102	N.C.
101	GND
100	N.C.
99	N.C.
98	GND
97	N.C.
96	N.C.
95	GND
94	N.C.
93	N.C.
92	GND
91	N.C.
90	N.C.
89	GND
88	TX1n
87	TX1p
86	GND
85	TX0n
84	TX0p
83	GND
82	N.C.
81	N.C.
80	GND
79	*(REFCLKn)*
78	*(REFCLKp)*
77	GND
76	N.C.
75	N.C.
74	GND
73	N.C.
72	N.C.
71	GND
70	N.C.
69	N.C.
68	GND
67	N.C.
66	N.C.
65	GND
64	N.C.
63	N.C.
62	GND
61	RX1n
60	RX1p
59	GND
58	RX0n
57	RX0p
56	GND
55	N.C.
54	N.C.
53	GND

	Top (4x50G)
104	GND
103	N.C.
102	N.C.
101	GND
100	TX3n
99	TX3p
98	GND
97	TX2n
96	TX2p
95	GND
94	N.C.
93	N.C.
92	GND
91	N.C.
90	N.C.
89	GND
88	TX1n
87	TX1p
86	GND
85	TX0n
84	TX0p
83	GND
82	N.C.
81	N.C.
80	GND
79	*(REFCLKn)*
78	*(REFCLKp)*
77	GND
76	N.C.
75	N.C.
74	GND
73	RX3n
72	RX3p
71	GND
70	RX2n
69	RX2p
68	GND
67	N.C.
66	N.C.
65	GND
64	N.C.
63	N.C.
62	GND
61	RX1n
60	RX1p
59	GND
58	RX0n
57	RX0p
56	GND
55	N.C.
54	N.C.
53	GND

	Top (6x50G)
104	GND
103	TX4n
102	TX4p
101	GND
100	TX3n
99	TX3p
98	GND
97	TX2n
96	TX2p
95	GND
94	TX5n
93	TX5p
92	GND
91	N.C.
90	N.C.
89	GND
88	TX1n
87	TX1p
86	GND
85	TX0n
84	TX0p
83	GND
82	N.C.
81	N.C.
80	GND
79	*(REFCLKn)*
78	*(REFCLKp)*
77	GND
76	RX4n
75	RX4p
74	GND
73	RX3n
72	RX3p
71	GND
70	RX2n
69	RX2p
68	GND
67	RX5n
66	RX5p
65	GND
64	N.C.
63	N.C.
62	GND
61	RX1n
60	RX1p
59	GND
58	RX0n
57	RX0p
56	GND
55	N.C.
54	N.C.
53	GND

	Top (8x50G)
104	GND
103	TX4n
102	TX4p
101	GND
100	TX3n
99	TX3p
98	GND
97	TX2n
96	TX2p
95	GND
94	TX5n
93	TX5p
92	GND
91	TX6n
90	TX6p
89	GND
88	TX1n
87	TX1p
86	GND
85	TX0n
84	TX0p
83	GND
82	TX7n
81	TX7p
80	GND
79	*(REFCLKn)*
78	*(REFCLKp)*
77	GND
76	RX4n
75	RX4p
74	GND
73	RX3n
72	RX3p
71	GND
70	RX2n
69	RX2p
68	GND
67	RX5n
66	RX5p
65	GND
64	RX6n
63	RX6p
62	GND
61	RX1n
60	RX1p
59	GND
58	RX0n
57	RX0p
56	GND
55	RX7n
54	RX7p
53	GND

Table 6: CFP2-DCO N x 25Gbit/s and 50Gbit/s Pin-Map

PIN#	NAME	I/O	Logic	Description
1	GND			
2	*(TX_MCLKn) or Vendor_Out0n*	O	CML	For optical waveform testing or Module vendor output
3	*(TX_MCLKp) or Vendor_Out0p*	O	CML	For optical waveform testing or Module vendor output
4	GND			
5	Vendor_In0n	I	CML	Module vendor input. Vendor specific.
6	Vendor_In0p	I	CML	Module vendor input. Vendor specific.
7	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
8	3.3V_GND			
9	3.3V			3.3V Module Supply Voltage
10	3.3V			
11	3.3V			
12	3.3V			
13	3.3V_GND			
14	3.3V_GND			
15	VND_IO_A	I/O		Module Vendor I/O A. Do Not Connect!
16	VND_IO_B	I/O		Module Vendor I/O B. Do Not Connect!
17	PRG_CNTL1	I	LVCMOS w/PUR	Programmable Control 1 set over MDIO, MSA Default: TRXIC_RSTn, TX & RX ICs reset, "0": reset, "1" or NC: enabled = not used
18	PRG_CNTL2	I	LVCMOS w/PUR	Programmable Control 2 set over MDIO, MSA Default: Hardware Interlock LSB, "00": ≤9W, "01": ≤12W, "10": ≤15W, "11" or NC: ≤18W = not used
19	PRG_CNTL3	I	LVCMOS w/PUR	Programmable Control 3 set over MDIO, MSA Default: Hardware Interlock MSB, "00": ≤9W, "01": ≤12W, "10": ≤15W, "11" or NC: ≤18W = not used
20	PRG_ALRM1	O	LVCMOS	Programmable Alarm 1 set over MDIO, MSA Default: HIPWR_ON, "1": module power up completed, "0": module not high powered up
21	PRG_ALRM2	O	LVCMOS	Programmable Alarm 2 set over MDIO, MSA Default: MOD_READY, "1": Ready, "0": not Ready.
22	PRG_ALRM3	O	LVCMOS	Programmable Alarm 3 set over MDIO, MSA Default: MOD_FAULT, fault detected, "1": Fault, "0": No Fault
23	GND			
24	TX_DIS	I	LVCMOS w/PUR	Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0" = transmitter enabled
25	RX_LOS	O	LVCMOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition
26	MOD_LOPWR	I	LVCMOS w/PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled
27	MOD_ABS	O	GND	Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host
28	MOD_RSTn	I	LVCMOS w/PDR	Module Reset. "0" resets the module, "1" or NC = module enabled, Pull Down Resistor in Module
29	GLB_ALRMn	O	LVCMOS	Global Alarm. "0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host

30	GND			
31	MDC	I	1.2V CMOS	Management Data Clock (electrical specs as per IEEE Std 802.3-2012)
32	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per IEEE Std 802.3-2012)
33	PRTADR0	I	1.2V CMOS	MDIO Physical Port address bit 0
34	PRTADR1	I	1.2V CMOS	MDIO Physical Port address bit 1
35	PRTADR2	I	1.2V CMOS	MDIO Physical Port address bit 2
36	VND_IO_C	I/O		Module Vendor I/O C. Do Not Connect!
37	VND_IO_D	I/O		Module Vendor I/O D. Do Not Connect!
38	VND_IO_E	I/O		Module Vendor I/O E. Do Not Connect!
39	3.3V_GND			
40	3.3V_GND			
41	3.3V			3.3V Module Supply Voltage
42	3.3V			
43	3.3V			
44	3.3V			
45	3.3V_GND			
46	3.3V_GND			
47	Vendor_In1n	I	CML	Module vendor input
48	Vendor_In1p	I	CML	Module vendor input
49	GND			
50	*(RX_MCLKn) or Vendor_Out1n*	O	CML	For optical waveform testing or Module vendor output
51	*(RX_MCLKp) or Vendor_Out1p*	O	CML	For optical waveform testing or Module vendor output
52	GND			

Table 7: CFP2-DCO Bottom Row Pin Description for N x 25Gbit/s applications

11 References

[1] www.cfp-msa.org

[2] CFP MSA Management Interface Specification, Version 2.6 r06a, March 27, 2017

[3] CFP MSA CFP2 Hardware Specification Revision 1.0, July 31, 2013

[4] CFP MSA CFPn Pin Allocation ver. 26

[5] OIF-MSA-100GLH-EM-01.1, September 20, 2011

[6] OIF-CEI-03.1, February 18, 2014

[7] IEEE P802.3-2015 Clause 83E (CAUI-4 C2M)

[8] ITU-T Recommendation G.709 (2016) Interfaces for the Optical Transport Network

[9] ITU-T Supplement G.sup58 (2017) Optical Transport Network Module Framer Interfaces

[10] IEEE P802.3bs-2017 Clause 120E (200GAUI-4 C2M and 400GAUI-8 C2M)

[11] OIF-CEI-56G-VSR-PAM4 Specifications

[12] CFP2 Hardware Baseline Design Rev. 1L

[13] IEEE P802.3bs-2017 Clause 120C (200GAUI-8 C2M and 400GAUI-16 C2M)

[14] IEEE P802.3by-2016 Clause 109B (25GAUI C2M)

[15] IEEE P802.3cd Clause 135C (LAUI-2 C2M)

[16] IEEE P802.3cd Clause 135E (50GAUI-2 C2M and 100GAUI-4 C2M)

[17] IEEE P802.3cd Clause 135G (50GAUI-1 C2M and 100GAUI-2 C2M)

12 Appendix A: Glossary

CFP C Form-factor Pluggable
DCO Digital Coherent Optical
OTN Optical Transport Network
MSA Multi-Source Agreement
MIS Management Interface Specification
NRZ None Return to Zero
PAM Pulse Amplitude Modulation
CEI Common Electrical I/O
VSR Very Short Reach
AUI Attachment Unit Interface
C2M Chip to Module

OTL Optical Transport Lane
FOIC FlexO Interface
MUX/DEMUX Multiplexer/Demultiplexer
IC Integrated Circuit
MDIO Management Data Input Output
MDC Management Data Clock
DC Direct Current
AC Alternating Current
MSB Most Significant Bit
LSB Last Significant Bit
Tx Transmitter
Rx Receiver
CML Current Mode Logic
RMS Root Mean Square

13 Appendix B: List of companies belonging to OIF when document is approved

Acacia Communications
ADVA Optical Networking
Alibaba
Amphenol Corp.
Analog Devices
Anritsu
Applied Optoelectronics, Inc.
Arista Networks
Barefoot Networks
BizLink Technology Inc.
Broadcom Limited
Cadence Design Systems
Cavium
CenturyLink
China Telecom Global Limited
Ciena Corporation
Cisco Systems
Corning
Credo Semiconductor (HK) LTD
Dell, Inc.
EFFECT Photonics B.V.
Elenion Technologies, LLC
Epson Electronics America, Inc.

eSilicon Corporation
Fiberhome Technologies Group
Finisar Corporation
Foxconn Interconnect Technology, Ltd.
Fujikura
Fujitsu
Furukawa Electric Japan
Global Foundries
Google
Hewlett Packard Enterprise (HPE)
Hitachi
Huawei Technologies Co., Ltd.
IBM Corporation
Infinera
Innovium
Inphi
Integrated Device Technology
Intel
Invecas, Inc.
IPG Photonics Corporation
JCRFO
Juniper Networks
Kandou Bus
KDDI Research, Inc.
Keysight Technologies, Inc.
Lightwave Logic
Lumentum
MACOM Technology Solutions
Marvell Semiconductor, Inc.
Maxim Integrated Inc.
MaxLinear Inc.
MediaTek
Mellanox Technologies
Microsemi Inc.
Microsoft Corporation
Mitsubishi Electric Corporation
Molex
Multilane SAL Offshore
NEC Corporation
NeoPhotonics

Nokia
NTT Corporation
O-Net Communications (HK) Limited
Oclaro
Orange
PETRA
Precise-ITC, Inc.
Qorvo
Ranovus
Renesas Electronics Corporation
Rianta Solutions, Inc.
Rockley Photonics
Rosenberger Hochfrequenztechnik GmbH & Co. KG
Roshmere
Samtec Inc.
Semtech Canada Corporation
SiFotonics Technologies Co., Ltd.
Sino-Telecom Technology Co., Inc.
Socionext Inc.
Spirent Communications
Sumitomo Electric Industries
Sumitomo Osaka Cement
Synopsys, Inc.
TE Connectivity
Tektronix
Telefonica SA
TELUS Communications, Inc.
UNH InterOperability Laboratory (UNH-IOL)
Verizon
Viavi Solutions Deutschland GmbH
Xelic
Xilinx
Yamaichi Electronics Ltd.